Problem 1.5. Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

a. Which processor has the highest performance expressed in instructions per second?

- Performance of P1 (instructions/sec) = $3 \times 10^9 / 1.5 = 2 \times 10^9$
- Performance of P2 (instructions/sec) = $2.5 \times 10^9 / 1.0 = 2.5 \times 10^9$
- Performance of P3 (instructions/sec) = $4 \times 10^9 / 2.2 = 1.8 \times 10^9$

b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

- Cycles(P1) = $10 \times 3 \times 10^9 = 30 \times 10^9$ s
- Cycles(P2) = $10 \times 2.5 \times 10^9 = 25 \times 10^9$ s
- Cycles(P3) = $10 \times 4 \times 10^9 = 40 \times 10^9$ s

- No. instructions(P1) = $30 \times 10^9 / 1.5 = 20 \times 10^9$
- No. instructions(P2) = $25 \times 10^9 / 1 = 25 \times 10^9$
- No. instructions(P3) = $40 \times 10^9 / 2.2 = 18.18 \times 10^9$

b. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

- CPI_{new} = CPI_{old} \times 1.2$, then CPI(P1) = 1.8, CPI(P2) = 1.2, CPI(P3) = 2.6

- $f = \text{No. instr.} \times \text{CPI/time}$, then
- $f(P1) = 20 \times 10^9 \times 1.8 / 7 = 5.14 \text{GHz}$
- $f(P2) = 25 \times 10^9 \times 1.2 / 7 = 4.28 \text{GHz}$
- $f(P1) = 18.18 \times 10^9 \times 2.6 / 7 = 6.75 \text{GHz}$

Problem 1.6. Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.

Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?
a. What is the global CPI for each implementation?

Class A: $10^5$ instr.
Class B: $2 \times 10^5$ instr.
Class C: $5 \times 10^5$ instr.
Class D: $2 \times 10^5$ instr.

Time = No. instr. × CPI/clock rate

Total time $P_1 = (10^5 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3) / (2.5 \times 10^9) = 10.4 \times 10^{-4}$s

Total time $P_2 = (10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2) / (3 \times 10^9) = 6.66 \times 10^{-4}$s

CPI($P_1$) = $10.4 \times 10^{-4} \times 2.5 \times 10^9 / 10^6 = 2.6$

CPI($P_2$) = $6.66 \times 10^{-4} \times 3 \times 10^9 / 10^6 = 2.0$

b. Find the clock cycles required in both cases.

clock cycles ($P_1$) = $10^5 \times 1 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3 = 26 \times 10^5$

clock cycles ($P_2$) = $10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2 = 20 \times 10^5$

Problem 1.12. Section 1.10 cites as a pitfall the utilization of a subset of the performance equation as a performance metric. To illustrate this, consider the following two processors. P1 has a clock rate of 4 GHz, average CPI of 0.9, and requires the execution of 5.0E9 instructions. P2 has a clock rate of 3 GHz, an average CPI of 0.75, and requires the execution of 1.0E9 instructions.

1.12.1 One usual fallacy is to consider the computer with the largest clock rate as having the largest performance. Check if this is true for P1 and P2.

T($P_1$) = No. instr. × CPI/clock rate

T($P_2$) = $10^9 \times 0.75 / (3 \times 10^9) = 0.25$s

clock rate ($P_1$) > clock rate($P_2$), performance($P_1$) < performance($P_2$)

1.12.2 Another fallacy is to consider that the processor executing the largest number of instructions will need a larger CPU time. Considering that processor P1 is executing a sequence of 1.0E9 instructions and that the CPI of processors P1 and P2 do not change, determine the number of instructions that P2 can execute in the same time that P1 needs to execute 1.0E9 instructions.

T($P_1$) = No. instr. × CPI/clock rate

T($P_2$) = $5 \times 10^9 \times 0.9 / (4 \times 10^9) = 1.125$s

T($P_2$) = $10^9 \times 0.75 / (3 \times 10^9) = 0.25$s

clock rate ($P_1$) > clock rate($P_2$), performance($P_1$) < performance($P_2$)

1.12.3 A common fallacy is to use MIPS (millions of instructions per second) to compare the performance of two different processors, and consider that the processor with the largest MIPS has the largest performance. Check if this is true for P1 and P2.
MIPS = Clock rate $\times 10^{-6}$/CPI
MIPS(P1) = $4 \times 10^9 \times 10^{-6/0.9} = 4.44 \times 10^3$
MIPS(P2) = $3 \times 10^9 \times 10^{-6}/0.75 = 4.0 \times 10^3$
MIPS(P1) > MIPS(P2), performance (P1) < performance (P2)

1.12.4 Another common performance figure is MFLOPS (millions of floating-point operations per second), defined as

MFLOPS = No. FP operations / (execution time $1E6$)

But this figure has the same problems as MIPS. Assume that 40% of the instructions executed on both P1 and P2 are floating-point instructions. Find the MFLOPS figures for the programs.

MFLOPS = No. FP operations $\times 10^{-6}/T$
MFLOPS(P1) = $0.4 \times 5E9 \times 1E - 6/1.125 = 1.78E3$
MFLOPS(P2) = $0.4 \times 1E9 \times 1E - 6/.25 = 1.60E3$
MFLOPS(P1) > MFLOPS(P2), performance(P1) < performance(P2)

Problem 1.14. Assume a program requires the execution of $50 \times 10^6$ FP instructions, $110 \times 10^6$ INT instructions, $80 \times 10^6$ L/S instructions, and $16 \times 10^6$ branch instructions. The CPI for each type of instruction is 1, 1, 4, and 2, respectively. Assume that the processor has a 2 GHz clock rate.

1.14.1 By how much must we improve the CPI of FP instructions if we want the program to run two times faster?

Clock cycles = CPI_{fp} \times No. FP instr. + CPI_{int} \times No. INT instr. + CPI_{branch} \times No. branch instr.
T_{CPU} = \text{clock cycles}/\text{clock rate} = \text{clock cycles}/2 \times 10^9
Clock cycles = 512 \times 10^6; T_{cpu} = 0.256s

To have the number of clock cycles by improving the CPI of FP instructions:

CPI_{improved fp} \times No. FP instr. + CPI_{int} \times No. INT instr. + CPI_{l/s} \times No. L/S instr. + CPI_{branch} \times No. branch instr. = \text{clock cycles }/2
CPI_{improved fp} = (\text{clock cycles}/2 - (CPI_{int} \times No. INT instr. + CPI_{l/s} \times No. L/S instr. + CPI_{branch} \times No. branch instr. ))/ No. FP instr.
CPI_{improved fp} = (256 - 462)/50 < 0 == not possible

1.14.2 By how much must we improve the CPI of L/S instructions if we want the program to run two times faster?

Using the clock cycle data from a.

To have the number of clock cycles improving the CPI of L/S instructions:

CPI_{fp} \times No. FP instr. + CPI_{int} \times No. INT instr. + CPI_{improved l/s} \times No. L/S instr. + CPI_{branch} \times No. branch instr. = \text{clock cycles }/2
CPI_{improved l/s} (\text{clock cycles}/2 - (CPI_{fp} \times No. FP instr. + CPI_{int} \times No. INT instr. + CPI_{branch} \times No. branch instr. )) / No. L/S instr.
CPI_{improved l/s} = (256 - 198)/80 = 0.725
1.14.3 By how much is the execution time of the program improved if the CPI of INT and FP instructions is reduced by 40% and the CPI of L/S and Branch is reduced by 30%?

$$\text{Clock cycles} = \text{CPI}_{\text{fp}} \times \text{No. FP instr.} + \text{CPI}_{\text{int}} \times \text{No. INT instr.} + \text{CPI}_{1/s} \times \text{No. L/S instr.} + \text{CPI}_{\text{branch}} \times \text{No. branch instr.}$$

$$\text{T}_{\text{CPU}} = \text{clock cycles/clock rate} = \text{clock cycles}/2 \times 10^9$$

$$\text{CPI}_{\text{int}} = 0.6 \times 1 = 0.6$$

$$\text{CPI}_{\text{fp}} = 0.6 \times 1 = 0.6$$

$$\text{CPI}_{1/s} = 0.7 \times 4 = 2.8$$

$$\text{CPI}_{\text{branch}} = 0.7 \times 2 = 1.4$$

$$\text{T}_{\text{CPU}}(\text{ before improv. }) = 0.256\text{s}$$

$$\text{T}_{\text{CPU}}(\text{ after improv. }) = 0.171\text{s}$$