Problem 2.1 (10). For the following C statement, what is the corresponding MIPS assembly code? Assume that the variables f, g, h, and i are given and could be considered 32-bit integers as declared in a C program. Use a minimal number of MIPS assembly instructions.
\[ f = g + (h - 5); \]

Answer:

```
addi f, h, -5 (note, no subi)
add f, f, g
```

Link: Why doesn’t there exists a subi opcode for MIPS?

Problem 2.3 (10). For the following C statement, what is the corresponding MIPS assembly code? Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively.

\[ B[8] = A[ij]; \]

Answer

```
sub $t0, $s3, $s4
add $t0, $s6, $t0
lw $t1, 16($t0)
sw $t1, 32($s7)
```

Problem 2.4 (10). For the MIPS assembly instructions below, what is the corresponding C statement? Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively.

```
sll $t0, $s0, 2 \quad // \quad t0 = f \times 4
add $t0, $s6, $t0 \quad // \quad t0 = &A[f]
sll $t1, $s1, 2 \quad // \quad t1 = g \times 4
add $t1, $s7, $t1 \quad // \quad t1 = &B[g]
lw $s0, 0($t0) \quad // \quad f = A[f]
```
addi $t2, $t0, 4
lw $t0, 0($t2)
add $t0, $t0, $s0
sw $t0, 0($t1)

Answer

Problem 2.9 (15). Translate the following C code to MIPS. Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively. Assume that the elements of the arrays A and B are 4-byte words:

Answer
sll $t0, $s3, 2 # $t0 <-- 4*i
add $t0, $t0, $s6 # $t0 <-- Addr(A[i])
lw $t0, 0($t0) # $t0 <-- A[i]
sll $t1, $s4, 2 # $t1 <-- 4*j
add $t1, $t1, $s6 # $t1 <-- Addr(A[j])
lw $t1, 0($t1) # $t1 <-- A[j]
add $t1, $t0, $t1 # $t1 <-- A[i] + A[j]
addi $t0, $s7, 32 # $t0 <-- Addr(B[8])
sw $t1, 0($t0) # B[8]<-- $t1

Problem 2.11 (25). For each MIPS instruction, show the value of the opcode (OP), source register (RS), and target register (RT) fields. For the I-type instructions, show the value of the immediate field, and for the R-type instructions, show the value of the destination register (RD) field.

Answer

<table>
<thead>
<tr>
<th></th>
<th>type</th>
<th>opcode</th>
<th>rs</th>
<th>rt</th>
<th>rd</th>
<th>immed</th>
</tr>
</thead>
<tbody>
<tr>
<td>addi $t0, $s6, 4</td>
<td>I-type</td>
<td>8</td>
<td>22</td>
<td>8</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>add $t1, $s6, $0</td>
<td>R-type</td>
<td>0</td>
<td>22</td>
<td>0</td>
<td>9</td>
<td></td>
</tr>
<tr>
<td>sw $t1, 0($t0)</td>
<td>I-type</td>
<td>43</td>
<td>8</td>
<td>9</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>lw $t0, 0($t0)</td>
<td>I-type</td>
<td>35</td>
<td>8</td>
<td>8</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>add $s0, $t1, $t0</td>
<td>R-type</td>
<td>0</td>
<td>9</td>
<td>8</td>
<td>16</td>
<td></td>
</tr>
</tbody>
</table>

Problem 2.22 (15). For the following C statement, write a minimal sequence of MIPS assembly instructions that does the identical operation. Assume $t1 = A$, $t2 = B$, and $s1$ is the base address of C.
A = C[0] << 4;

Answer
Problem 2.23 (15). Assume $t0 holds the value 0x00101000. What is the value of $t2 after the following instructions?

```
slt $t2, $0, $t0
bne $t2, $0, ELSE
j DONE
ELSE:  addi $t2, $t2, 2
DONE:
```

Answer

$t2 = 3