High Speed Digital Design Principles

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**Background**

All embedded Intel® architecture products vary in their uses, but they have one thing in common: the complexity of their design. From an engineer's perspective there are many new and unfamiliar challenges of getting large amounts of electrical, electronic hardware on generally a smaller piece of board/PCB in the case of embedded design.

This white paper discusses some of the major factors that need to be considered in designing an embedded product and the various high speed digital design concepts that play a vital role in the functionality of the hardware/ product as a whole. This paper will help a designer understand why the electrical signals act so differently on a high speed design, identify the various problems that may occur in the design, and solve these problems.

**Groundwork**

In the world of high speed digital design and architecture the following concepts play a major role in deciding the success of a product.

First the architecture of a system forms an important part of the design equation. Next, designers must get through the schematics and layout of the design. During the layout phase the signal integrity factors such as reflections, ground bounce, crosstalk, power supply noise and EMI factors such as radiation and electrostatic discharge need to be considered before the board is built. The guidelines necessary for the optimal schematic and layout design of the board are provided through the schematic and layout checklists in the product Platform Design Guideline (here on referred to as the PDG).

For a good design a lot of ground work is done before the actual board is built. This is made up of system architecture, schematics and layout of the design.

**Get Me An Architect!**

The first step towards a good design is the system architecture. Knowing the parts that make up your complete system and laying them out on a board using computer aided software will help visualize what the board will end up looking like. Be sure to keep memory, CPU, MCH sections separate from the ICH and IO sections. This will help create a clean design. This first step ensures that the designer will have a plan to work with when doing schematics and layout of devices. Figure 1 shows a sample board which employs a clean design technique.
Figure 1 illustrates a design which employs a good architecture and layout method by following the product PDG.

“Schematic”-ally Correct

It is important to check the schematics against the guidelines provided for various high speed busses (Clock signals, DDR2, DDR3, PCI express etc) and to correct the errors. It is also imperative that all the pull up/pull down resistors are verified for the value and the voltages provided to the devices are checked. Additional information on schematic design and the process of checking schematics is available in the Embedded Design Center (EDC).

Schematics need to be thoroughly checked since layout is directly cascaded down from the schematics. A small error in the schematic will be harder to find in layout. Layout engineers do not check for the right values; they layout the schematic reports.
What’s with the “Layout”?

High speed signal principles are put to use in the layout stage. This stage defines how the copper wires on the PCB are cut into traces of stripline and microstrip. All the devices are also placed on the board either on the top or bottom layer and interconnections are made through an intensely woven inner layer of signals.

Layout is another stage during the design where the principles play a vital role. Most of the principles can be followed in a general manner in the architecture and schematic steps, but during layout the high speed design principles are used in every signal route.

Theory

*Theory: speculation, knowledge, methodologies and mathematical proof (Source: Wikipedia)*

The word “theory” describes high speed design principles as they have evolved though speculation, knowledge, furthered by mathematical proof and then using systematic study and methodology.

Gordon Moore stated “It can’t continue forever. The nature of exponentials is that you push them out and eventually disaster happens”. We are seeing more of this happening as the speed is pushed for many digital interfaces. We are looking to multiply cores to make devices use parallel processing rather than brute force speed. This in turn has made the devices more complicated but has not changed the principles on a system design level drastically.

That said, the principles used in high speed digital design are countless, and many authors have put forward their theories and findings about the peculiar way electrical signals behave as the frequency of operation gets closer to the gigahertz range. The following sections will try to shed light on a few of the major principles used in high speed design.

To Be the “Signal” or Not To Be the “Signal”

Signals in high speed design are electrical in nature and consist of current flowing through the wires. The following principles of mutual inductance, mutual capacitance and crosstalk will affect the response, quality of the electrical signal when it flows through a copper trace (essentially a transmission line).

The schematic only shows the path the signal path from a source to a destination. It hides the fact that when signal flows there are two attributes:
The current forms loops in circuit. These loops are sometimes simple or can be complex. Every loop of current has inductance $L$ associated with it. A series inductor passes DC but blocks high frequency noise.

Given a value of $L$ and also given the frequency $f$, then for a sinusoidal input the equation that governs that effective impedance magnitude is given by:

$$X_l = 2 \cdot (\pi) \cdot f(frequency) \cdot L \quad (Source: \ HSDD \ 2007 \ V.13)$$

From the equation we see that with the increasing frequency of systems the effective impedance of the given circuit increases. Thus a good high speed design would need to provide as little of an inductance value in the circuit to provide a good signal quality.

**Figure 2** shows the effect of current loops causing *mutual inductance*.

**Figure 2. Mutual Inductance (Source: High Speed Digital Design 2007 V .13)**

Two conductors in close proximity to each other, carrying a signal, share an electric field and this electric field causes an unintentional current flow between them. The coupling between them acts like a shunt capacitor. A capacitor blocks DC but passes high frequency signals. Given the value of $C$ and frequency $f$, then for a sinusoidal input the equation that governs the effective impedance is given by

$$X_c = \frac{1}{2 \cdot \pi \cdot f \cdot C} \quad (Source: \ HSDD \ 2007 \ V.13)$$
The equation shows that the effective capacitive of the circuit starts to decrease as the frequency of the circuit gets higher. This means that capacitors start becoming more like short circuits at higher frequencies.

Figure 3 shows the how mutual capacitance is created in circuits of close proximity.

**Figure 3. Mutual Capacitance (Source: High Speed Digital Design 2007 V .13)**

These properties can help us find the effective capacitance or inductance present in a circuit due to mutual inductance and capacitance. These are the parasitic elements involved in a circuit and they have the ability to destroy a good frequency response.

It has already been stated that current flows in loops, these loops form the return path. The problem with high speed digital design is that current bunches together and forms very tight loops that try to follow the path as close as possible. Figure 4 shows this property of current.

**Figure 4. Current Loops (Source: High Speed Digital Design 2007 V .13)**
Figure 4 demonstrates that this poses a serious problem for a designer. Unless there is a proper return path for high speed signals, the return current will flow through a longer return path forming a larger loop and this can cause signal issues on the signal and also other signals due to the mutual inductance caused.

Experience shows that for a high speed digital design that uses low impedance devices and high currents in the circuit designers need to be concerned about mutual inductance. A mutual inductance can cause either a positive or negative edge crosstalk on another signal based on the direction of the loop present and the duration equal to the rise time of the aggressive signal. Mutual capacitance, not playing a major factor in the high speed designs, generally causes a positive edge crosstalk with duration equal to the rise time of the aggressive signal.

“**I’ll be back**” – the “**Termination**”

The signals on a board are transmitted using copper traces; these are essentially transmission lines. Characteristic impedance is one of the properties of transmission lines.

*Characteristic impedance* is the ratio of voltage to current in a transmission line. The instant a signal propagates the transmission line, the input impedance of the PCB trace looks resistive. The PCB trace impedance is a value that needs special attention from a designer. It is difficult to match the load and the source in complex designs. But in theory a perfectly matched transmission line will be devoid of any reflections from the far end and thereby will not have any reflected signal causing an addition or subtraction to the original signal at the near end and so on. Reflections can cause ringing of the signal. If the signal has enough time to settle to its final value after all the reflections before the next transition the design will not encounter issues. If the time is not adequate then there might be an error to the value that is found due to the reflections.

Reflections on a transmission line can be avoided by using terminations to the transmission line. The most popular terminations used in the digital logic are either end termination or series termination. End terminations use a resistor or split a pair of resistors which connect to VCC and ground respectively with the line as the reference point. Figure 5 shows the end termination topology on a transmission line near the load with a split resistor termination.
The second most common method of terminations is the one used in point to point signals. This is the **series termination**. A resistor of matched value to the impedance of the line is put in series to the source before the transmission line. The resistor accomplishes the cancellation of reflections as shown in Figure 6.

There are also other types of terminations:

1. AC with DC balance terminations – used with clock signals
2. AC without DC balance terminations
3. Double series termination

For additional information on terminations, refer to
Shhh...No “Noise” Please!

The biggest roadblock for any high speed design is noisy signals. With added noise comes the problem of having more errors on a given bus. This sometimes can be such a huge issue that the system design might have to go through a layout change to get it resolved. This can cost a lot of money and time.

As seen previously, the concepts of mutual inductance and capacitance cause a majority of the crosstalk which results in noise being injected on the signal. A few simple rules keep the noise from becoming the nemesis of the design.

1. Provide ample spacing as required (or as provided in the PDG, PCI-sig specs, Jedec specs) between pairs of high speed signals.
2. Provide ample ground planes to guarantee a quick return path for the high speed signal currents. This avoids the unwanted looping effect if no ground planes are provided.
3. Provide ample stitching capacitors (decoupling) for high speed signals if they cross planes. These provide a return path to the reference plane.
4. Use the right termination; this kills the reflections and crosstalk.
5. Avoid having slots on the ground plane. This causes unwanted current loops to interact with other sensitive circuits.
6. With connector pins make sure to have enough clear ground cut outs around the pins to provide a return path.
7. Use a good stack up for the design, alternate signal layers with ground and power planes.
8. Provide a separate region on your board to house all the sensitive analog circuits away from the high speed digital circuits.

The “Scope” of the Issue – Debug Techniques

One can expect to go through at least two revisions of a design before production. Murphy’s Law states that "Whatever can go wrong will go wrong, and at the worst possible time, in the worst possible way". Not going that far we can safely assume that there is always a chance that errors can occur and would need to be debugged in a high speed design. A favorite tool in the lab that any electrical engineer will swear by is the oscilloscope.

Many kinds of scopes and probes exist and most of them can measure an electrical signal. The problem is most engineers assume that the picture on
the scope is the way the signal actually is behaving. The following types of probes exist in the realm of measurement equipment.

1. **10x 10-pF Passive Probe**

   The probe works on signals of about 300MHz. This is too slow for most high speed signals. Figure 7 shows the internals of this probe.

   **Figure 7. Passive Probe (Source: High Speed Digital Design 2007 V.13)**

   ![](passive_probe.png)

2. **FET-Input Probe**

   The FET amplifier separates the input circuit from the cable effects. This probe has higher bandwidth capability of up to 6GHz. The tips do get warm due to the power dissipation. Figure 8 shows the FET amplifier.

   **Figure 8. FET-Input Probe (Source: High Speed Digital Design 2007 V.13)**

   ![](fet_input_probe.png)
3. Differential Active Probes.

They have high input impedance of almost up to 250-300 ohms and higher bandwidth.

4. Resistive Input Probes.

These are inexpensive and offer higher bandwidth as the differential probes. The problem is this probe works only with low impedance circuits.

A designer/engineer should research the type of probe to be used based on the type of signal. If a fast signal is measured using a passive probe the rise times reported are different compared to measuring it using the right bandwidth probe.

The equation that defines a measurement setup is as follows

$$T_{\text{display}} = (T_{\text{probe}}^2 + T_{\text{scope}}^2)^{1/2}$$

For example a 5GHz probe with a 5GHz scope would yield a system capable of measuring a 3.5GHz signal.

We Researched It, We Designed It, and It Works!

This paper is but a short introduction to the world of high speed design. It attempts to answer some of the basic questions that come to an engineer’s mind when designing an embedded Intel® architecture product using high speed principles.

For more information on high speed digital design principles, refer to the publications listed in
For more information on Embedded products with Intel® architecture, go to the [Embedded Design Center (EDC)](Embedded Design Center (EDC)) webpage.
References


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5. PCB Design for Real-World EMI Control (The Springer International Series in Engineering and Computer Science), Bruce R. Archambeault, James Drewniak
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Acronyms/Keywords

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<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tr>
<td>AC</td>
<td>Alternating Current</td>
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<tr>
<td>DC</td>
<td>Direct Current</td>
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<td>FET</td>
<td>Field Effect Transistor</td>
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<td>Ghz</td>
<td>Giga hertz</td>
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<td>PDG</td>
<td>Platform Design Guide</td>
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<td>pF</td>
<td>Pico Farad</td>
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<tr>
<td>VCC</td>
<td>Power source</td>
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<tr>
<td>XI</td>
<td>Effective inductance of the circuit</td>
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<tr>
<td>Xc</td>
<td>Effective capacitance of the circuit</td>
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<tr>
<td>Zo</td>
<td>Characteristic impedance of the transmission line</td>
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