# CSE 5356 System on Chip Design
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# EE 5315 System on Chip Design
# EE 4328 Current Topics in Electrical Engineering
## Fall 2022
**(subject to change prior to the first day of class)**

## Instructor Information

**Instructor:**
Jason Losh, Ph.D.

**Office Number:**
ERB 649

**Office Telephone Number:**
+1 817-272-3785 (CSE Department)

**Email Address:**
jlosh@uta.edu

**Faculty Profile:**
https://mentis.uta.edu/explore/profile/jason-losh

**Office Hours:**
Office hours will be held before and after each class, since this time is most convenient to students. Office hours are also available by appointment.

**Teaching Assistants:**
Due to the requirement that this syllabus be posted 30 days before the beginning of classes, no TA information is available. This will be given out during the first day of class and is not part of the syllabus.

## Course Information

**Section Information:**
CSE 4356-001, CSE 5356-001, EE 4328-002, and EE 5315-001

**Time and Place of Class Meetings:**
TTh 2:00 to 3:20 pm, ERB 131
This is a 100% face-to-face course. This is not an online course.

**Description of Course Content:**
Programming and implementation of FPGA-based system on chip solutions, including processor subsystems, FPGA fabric, processor to FPGA bridges, and device drivers. Prerequisite: CSE 3442, CSE 5400, or consent of instructor.

**Student Learning Outcomes:**
Upon successful completion of this course, students will have knowledge of:

- Knowledge of the architecture of FPGA-based SoC solutions
- Differences between soft- and hard-processor subsystems (HPS)
- Survey of common hard-processor subsystems

- Detailed knowledge of the DE1 SoC development board and environment
- Functional knowledge of the Quartus development platform
- Review of Verilog coding
- Development, coding, and testing of FPGA-only solutions
- Development, coding, and testing of HPS-only solutions
- Creating bridges from the processor to the FPGA fabric
- Designing CPU-accessible peripherals
- Designing clock-crossing with multiple and asynchronous clock domains
- Write Linux virtual memory and virtual file system interfaces
- Writing Linux device drivers for FPGA access
- Developing SoC real-world applications

**Class Web Page:**
Additional files will be provided at http://ranger.uta.edu/~jlosh/.

**Communication:**
All class-wide communication by the instructor, including distribution of homework sets, will occur via the class listserv. If you are enrolled prior to the first day of class, you will be added to the listserv automatically. If you add on or after the first day of class, please sign up for the CSE4356-L listserv by sending an e-mail from your UTA e-mail account to listserv@listserv.uta.edu from your UTA e-mail account (no subject line needed) and the command SUBSCRIBE CSE4356-L as the message body. You will then receive an e-mail from the listserv server to which you must acknowledge to join the listserv with "OK" in an e-mail.

**Textbooks and Other Course Materials:**
Extensive references, datasheets, application notes, and class notes will be provided on the course web site at http://ranger.uta.edu/~jlosh/.

Students will checkout a DE1-SoC kit and Analog Discovery 2 kit for the semester on Friday, August 26. These kits must be returned after the project defense on Tuesday, December 6 to prevent a grade and financial hold.

**Major Assignments and Examinations:**
Labs: Various lab assignments will be made during the semester.
Test: Thursday, November 17
Project: Tuesday, December 6

**Technology Requirements:**
Students will need a computer capable of running Intel Quartis Prime Lite 20.1.1.

## Grading Information

**Grading:**
- Grade scale: A (90-100), B (80-89), C (70-79), D (60-69), and F (0-59)
- Grade calculation: Labs (35%), Test (25%), Project (40%)
- The instructor reserves the right to make reasonable changes in performance evaluation as needed.
- Any request for re-grading must be submitted to the Grader within one week of the completion of grading. If, after requesting a re-grade from the Grader and getting a response, you may refer the case to the instructor iif you think further action is needed.

**Expectations for Out-of-Class Study:**
As a general rule of thumb, for every credit hour earned, a student should spend 3 hours per week working outside of class. Hence, for this 3-credit course, a minimum expectation of 9 hours of study is expected in addition to the time spent in lecture.

**Test:**

- To ensure that all students are treated equally and given the same time to prepare for the exam, no makeup will be provided for any test missed.
- If you know you are going to miss the test, you can request an advance test given 1 week prior to the normally scheduled time for the exam, with the understanding that any curve applied to the test taken at the official test time will not apply to the advance test, since the content of that test will be unique.
- The test is on-campus
- The test is open-book, open-notes, calculators allowed.

**Labs:**

- Labs are individual assignments. Discussing lab topics is allowed, but the submissions must be unique. Sharing of code is not allowed.

**Project:**

- The projects will consist of hardware construction and firmware development and it is expected that it will take approximately 80 hours to complete.
- Projects teams will consist of 1 or 2 students. Discussing project topics is allowed, but the submissions must be unique to the team. Sharing of code is not allowed.
- Interim deadlines for hardware construction and some software milestones will occur as part of the lab exercises.

## Course Schedule

The anticipated lecture order is as follows:

- Syllabus overview, course objectives, course resource requirements (1 hr)
- Discussion of DE1-SoC kit and check out. (0.5 hrs)
- Review of combinational logic, Verilog, and Quartus. (1.5 hrs)
- Review of sequential logic, Verilog, and Quartus (3 hrs)
- Designing registers and register stacks (1.5 hrs)
- Designing FIFO buffers (1.5 hrs)
- Designing counters and frequency dividers (1.5 hrs)
- Designing clocks and timers (1.5 hrs)
- Project introduction, selection of teams (0.5 hrs)
- Project-specific lecture (SERDES design) (1.5 hrs)
- Memory mapped interface (1 hr)
- Using the Quartus Platform Designr=er (was Qsys) (1.5 hr)
- Designing a memory-mapped register interface (1.5 hrs)
- Case study: Designing a GPIO peripheral (2 hrs)
- Case study: Designing a quadrature encoder peripheral with multiple clock domains (2 hrs)
- Case study: Designing a PWM peripheral (2 hrs)
- Virtual memory interface (/dev/mem) (1 hr)
- Virtual file system (/sys/class/*) kernel module design (1.5 hrs)
- Higher-level kernel modules (1 hr)
- Interrupts in Linux (1 hr)
- Project-specific lectures (2.5 hrs)
- Test (1.5 hrs)

The instructors reserve the right to make changes in the schedule as needed as the class progresses.

The official dates for registration, census, and dropping are available at www.uta.edu/acadcal.

## Academic Integrity

This information is copied from http://www.uta.edu/conduct/academic-integrity/index.php.

The University of Texas at Arlington strives to uphold and support standards of personal honesty and integrity for all students consistent with the goals of a community of scholars and students seeking knowledge and responsibility. Furthermore, it is the policy of the University to enforce these standards through fair and objective procedures governing instances of alleged dishonesty, cheating, and other academic/non-academic misconduct.

Scholastic dishonesty includes, but is not limited to, cheating, plagiarism, and collusion on an examination or an assignment being offered for credit. Each student is accountable for work submitted for credit, including group projects.

- Cheating
  - Copying another's test or assignment (added note: remember this includes homework!)
  - Communication with another during an exam or assignment (i.e. written, oral or otherwise)
  - Giving or seeking aid from another when not permitted by the instructor
  - Possessing or using unauthorized materials during the test
  - Buying, using, stealing, transporting, or soliciting a test, draft of a test, or answer key
- Plagiarism
  - Using someone else's work in your assignment without appropriate acknowledgement
  - Making slight variations in the language and then failing to give credit to the source
- Collusion
  - Without authorization, collaborating with another when preparing an assignment

## Institution Information

UTA students are encouraged to review the below institutional policies and informational sections and reach out to the specific office with any questions. To view this institutional information, please visit the Institutional Information page (http://www.uta.edu/provost/administrative-forms/course-syllabus/index.php) which includes the following policies among others:

- Drop Policy
- Disability Accommodations
- Title IX Policy
- Academic Integrity
- Student Feedback Survey
- Final Exam Schedule

## Additional Information

**Face Covering Policy:**
While face coverings are not mandatory, all students and instructional staff are welcome to wear face coverings while they are on campus or in the classroom.

**Attendance:**
At The University of Texas at Arlington, taking attendance is not required but attendance is a critical indicator of student success. Each faculty member is free to develop his or her own methods of evaluating students' academic performance, which includes establishing course-specific policies on attendance. However, while UT Arlington does not require instructors to take attendance in their courses, the U.S. Department of Education requires that the University have a mechanism in place to

mark when Federal Student Aid recipients "begin attendance in a course." UT Arlington instructors will report when students begin attendance in a course as part of the final grading process. Specifically, when assigning a student a grade of F, faculty report must the last date a student attended their class based on evidence such as a test, participation in a class project or presentation, or an engagement online via Canvas. This date is reported to the Department of Education for federal financial aid recipients.

In this course, attendance in-class, on-campus is expected. Attending tests and laboratories in person is required.

**Emergency Exit Procedures:**
Should we experience an emergency event that requires evacuation of the building, students should exit the room and move toward the nearest exit. When exiting the building during an emergency, do not take an elevator but use the stairwells instead. Faculty members and instructional staff will assist students in selecting the safest route for evacuation and will make arrangements to assist individuals with disabilities.

**Academic Success Center**
The Academic Success Center (ASC) includes a variety of resources and services to help you maximize your learning and succeed as a student at the University of Texas at Arlington. ASC services include supplemental instruction, peer-led team learning, tutoring, mentoring and TRIO SSS. Academic Success Center services are provided at no additional cost to UTA students. For additional information visit: Academic Success Center. To request disability accommodations for tutoring, please complete this form.

## Emergency Phone Numbers

In case of an on-campus emergency, call the UT Arlington Police Department at **817-272-3003** (non-campus phone), **2-3003** (campus phone). You may also dial 911. Non-emergency number 817-272-3381