CSE 5356 System on Chip Design
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EE 5315 System on Chip Design
EE 4328 Current Topics in Electrical Engineering
Fall 2023
(subject to change prior to the first day of class, revised 8/20)

Instructor Information

Instructor:
Jason Losh, Ph.D.

Office Number:
ERB 649 (office hours will be held in the ERB 121-126 lab area)

Office Telephone Number:
+1 817-272-3785 (CSE Department)

Email Address:
jlosh@uta.edu

Faculty Profile:
https://mentis.uta.edu/explore/profile/jason-losh

Office Hours:
Office hours will be held before and after each class, since this time is most convenient to students. Office hours are also available by appointment.

Teaching Assistants:
Boddu Mourya Chandra, mxb2108@mavs.uta.edu

Course Information

Section Information:
CSE 4356-001, CSE 5356-001, EE 4328-002, and EE 5315-001

Time and Place of Class Meetings:
TTh 5:30 to 6:50 pm, ERB 131
This is a 100% face-to-face course. This is not an online course.

Description of Course Content:
Programming and implementation of FPGA-based system on chip solutions, including processor subsystems, FPGA fabric, processor to FPGA bridges, and device drivers. Prerequisite: CSE 3442, CSE 5400, or consent of instructor.

Student Learning Outcomes:
Upon successful completion of this course, students will have knowledge of:

- Knowledge of the architecture of FPGA-based SoC solutions
- Differences between soft- and hard-processor subsystems
- Survey of common hard-processor subsystems
- Detailed knowledge of the Xilinx XUP Blackboard development board and environment

- Functional knowledge of the Vivado development platform
- Review of System Verilog coding with behavioral modeling style
- Development, coding, and testing of FPGA-only solutions
- Development, coding, and testing of PS-only solutions
- Creating bridges from the processor to the FPGA fabric
- Designing CPU-accessible peripherals
- Designing clock-crossing with multiple and asynchronous clock domains
- Write Linux virtual memory and virtual file system interfaces
- Writing Linux device drivers for FPGA access
- Developing SoC real-world applications

Class Web Page:
Additional files will be provided at http://ranger.uta.edu/~jlosh/.

Communication:
All class-wide communication by the instructor, including distribution of homework sets, will occur via the class listserv. If you are enrolled prior to the first day of class, you will be added to the listserv automatically. If you add on or after the first day of class, please sign up for the CSE4356-L listserv by sending an e-mail from your UTA e-mail account to listserv@listserv.uta.edu from your UTA e-mail account (no subject line needed) and the command SUBSCRIBE CSE4356-L as the message body. You will then receive an e-mail from the listserv server to which you must acknowledge to join the listserv with "OK" in an e-mail.

Textbooks and Other Course Materials:
Extensive references, datasheets, application notes, and class notes will be provided on the course web site at http://ranger.uta.edu/~jlosh/.

For the CSE students, an SoC board can be checked out for the semester. The SoC board must be returned after the project defense on Tuesday, December 5 to prevent a grade and financial hold.

For EE students, we are working to see if boards can be purchased for check out. The academic price of the board is around $139 if the board needs to be purchased. More information will be provided as soon as possible.

Students may also checkout an Analog Discovery 2 kit for the semester on Thursday, August 24. These kits must be returned after the project defense on Tuesday, December 5 to prevent a grade and financial hold. In lieu of checking out an Analog Discovery 2 kit, you can also use the 4-channel 200 MHz scopes with the I2C/SPI/UART debug personality in ERB 126.

Major Assignments and Examinations:

Labs:	Various lab assignments will be made during the semester.
Test:	Thursday, November 16
Project:	Wednesday, November 29

Technology Requirements:
Students will need a computer capable of running Vivado.

Grading Information

Grading:
- Grade scale: A (90-100), B (80-89), C (70-79), D (60-69), and F (0-59)
- Grade calculation: Labs (35%), Test (25%), Project (40%)
- The instructor reserves the right to make reasonable changes in performance evaluation as needed.

- Any request for re-grading must be submitted to the Grader within one week of the completion of grading. If, after requesting a re-grade from the Grader and getting a response, you may refer the case to the instructor iif you think further action is needed.

Expectations for Out-of-Class Study:
As a general rule of thumb, for every credit hour earned, a student should spend 3 hours per week working outside of class. Hence, for this 3-credit course, a minimum expectation of 9 hours of study is expected in addition to the time spent in lecture.

Test:
- To ensure that all students are treated equally and given the same time to prepare for the exam, no makeup will be provided for any test missed.
- If you know you are going to miss the test, you can request an advance test given 1 week prior to the normally scheduled time for the exam, with the understanding that any curve applied to the test taken at the official test time will not apply to the advance test, since the content of that test will be unique.
- The test is on-campus
- The test is open-book, open-notes, calculators allowed.

Labs:
- Labs are individual assignments. Discussing lab topics is allowed, but the submissions must be unique. Sharing of code is not allowed.
- You should complete and submit each lab assignment by the deadline given in class. There is a 20% reduction in credit for each week day that the lab assignment is late.

Project:
- The projects will consist of hardware construction and firmware development and it is expected that it will take approximately 80 hours to complete.
- Projects teams will consist of 1 or 2 students. 6000-level students will work in teams of one.
- Discussing project topics is allowed, but the submissions must be unique to the team. Sharing of code is not allowed.
- Interim deadlines for hardware construction and some software milestones will occur as part of the lab exercises.
- While the lecture content of this course is shared across multiple courses, students enrolled in a graduate course will have additional project components assigned.

Course Schedule

Since there has not been a semester in many years without canceled course days, this is the anticipated lecture order without fixed dates:

- Syllabus overview, course objectives, course resource requirements (1 hr)
- Discussion of Xilinx XUP Blackboard and check out. (0.5 hrs)
- Review of combinational logic in Vivado. (1.5 hrs)
- Review of sequential logic with behavioral modeling in Vivado (3 hrs)
- Designing registers and register stacks (1.5 hrs)
- Designing FIFO buffers (1.5 hrs)
- Designing counters and frequency dividers (1.5 hrs)
- Designing clocks and timers (1.5 hrs)
- Project introduction, selection of teams (0.5 hrs)
- Memory mapped interface (1 hr)
- Using the Block Designer (1.5 hr)
- Designing a memory-mapped register interface (1.5 hrs)
- Case study: Designing a GPIO peripheral (2 hrs)
- Virtual memory interface (/dev/mem) (1 hr)

- Virtual file system (/sys/class/*) kernel module design (1.5 hrs)
- Interrupts in Linux (1 hr)
- Case study: Designing a quadrature encoder peripheral with multiple clock domains (2 hrs)
- Case study: Designing a PWM peripheral (2 hrs)
- Higher-level kernel modules (2 hrs)
- Project-specific lectures (4 hrs)
- Test (1.5 hrs)

The instructor reserves the right to make changes in the schedule as needed as the class progresses. When the class project is chosen, this will also result in an altered lecture order.

The official dates for registration, census, and dropping are available at www.uta.edu/acadcal.

Academic Integrity

This information is copied from http://www.uta.edu/conduct/academic-integrity/index.php.

The University of Texas at Arlington strives to uphold and support standards of personal honesty and integrity for all students consistent with the goals of a community of scholars and students seeking knowledge and responsibility. Furthermore, it is the policy of the University to enforce these standards through fair and objective procedures governing instances of alleged dishonesty, cheating, and other academic/non-academic misconduct.

Scholastic dishonesty includes, but is not limited to, cheating, plagiarism, and collusion on an examination or an assignment being offered for credit. Each student is accountable for work submitted for credit, including group projects.

- Cheating
  - Copying another's test or assignment (added note: remember this includes homework!)
  - Communication with another during an exam or assignment (i.e. written, oral or otherwise)
  - Giving or seeking aid from another when not permitted by the instructor
  - Possessing or using unauthorized materials during the test
  - Buying, using, stealing, transporting, or soliciting a test, draft of a test, or answer key
- Plagiarism
  - Using someone else's work in your assignment without appropriate acknowledgement
  - Making slight variations in the language and then failing to give credit to the source
- Collusion
  - Without authorization, collaborating with another when preparing an assignment

Safety Rules for ERB 121-127 and 132 Labs:

Scope:
- All UTA safety rules and regulations must be followed.
- These rules are in addition to UTA lab safety rules.
- In the event that a rule contained below is in conflict with UTA lab safety rules, the UTA safety rules shall supersede.

General rules:
- Students can only be in the lab when a teaching assistant (TA), faculty member, or staff member is present.
- Students should be professional at all times in the lab.

- Food is not allowed in the lab at any time. Drinks, including those in sealed container, is not allowed in the lab. The only exception to this rule in the marked tables in ERB 125.
- When leaving the lab, all work surfaces and floors should be clear of breadboards, cables, wires, and tools prior to leaving.
- When leaving the bench, turn off all lab equipment and unplug soldering irons.
- When leaving the bench, make sure that all cables, tools, and soldering equipment are properly stored in the correct location.
- Please ensure that the lab is kept in a neat and tidy manner.
- Please pick up any loose wires or parts on the bench and floor before leaving the lab.
- Note any hazards observed in the lab to the TA, faculty, or staff member immediately.
- For test equipment incorporating multi-language menus, such as oscilloscopes, please return the language to English before leaving the bench.
- When returning parts that are not consumables, make certain that the parts are returned to the correct drawer. If you are not certain, please leave them with the TA, faculty member, or staff member.
- Students should store backpacks and similar items in a way that does not create a trip hazard to others. In ERB 126 and 127, there are cabinet spaces at the base of the benches for this purpose.

Soldering irons:

- Soldering must be performed in the labs only at the soldering benches. Never solder in dorm rooms.
- Soldering irons should be used with care, while wearing safety glasses, and only after receiving training.
- When soldering and removing parts, or reworking a board, please use special care to ensure that solder is not splattered.
- Soldering irons must be placed back in their soldering station holder when not soldering to prevent the chance or injury or fire.
- Please keep the soldering station sponges wet when cleaning the iron tip but ensure that water is not spilled on the floor creating a slip hazard.
- Use the soldering iron smoke absorber fan units when soldering. Use them in the horizontal position (air exits upward) to prevent directing air flow across the table into the face of another user.
- Some solders can contain lead, so wash hands thoroughly after using the soldering irons. No eating or drinking is allowed at the soldering benches. The green solder spools in the lab generally indicate a lead-free solder.
- No self-contained butane soldering irons are permitted.
- Wear appropriate personal protection equipment (PPE).

Chemicals and lasers:

- In labs where chemicals or lasers are used, students and faculty must receive the appropriate safety training prior to working in the lab.
- In labs with chemicals, consult the safety data sheet (SDS) folder for information.
- Wear appropriate personal protection equipment (PPE) at all times.
- If transferring chemicals to secondary containers, clearly mark the contents of the container. Specially, a label with spelled out chemical name and hazards is required. Also, for water bottles, label as “not for human consumption on the bottle.” A green dot can also be attached to indicate that the chemical is not hazardous.

Hand tools:

- Hand tools must be used with care and only when safety glasses are being worn.
- Diagonal cutters in particular can create tension on the wires during the cutting process, ejecting the loose wire, so please use special care.
- Wear appropriate personal protection equipment (PPE).

Power tools:

- Short time use of small powered cutting tools such as a drill/driver can only be used at the soldering tables using a backup board to prevent damage to the tables.
- For extended machining tasks, please use the designated Makerspace areas that are designed to handle the additional safety requirements and dust inhalation hazards.
- Wear appropriate personal protection equipment (PPE).
- Jewelry, necklaces, and lanyards should be removed.
- Long hair should be tied back to prevent being caught in the tool.
- For labs with drill presses, band saws, laser cutters, CNC machines, and similar equipment, students must take the appropriate safety trainiafng prior to using the equipment.

Electrical hazards:

- The labs for these classes generally use voltages of 32V or less, but care must always be shown in using electrical circuits, regardless of the voltage.
- Do not use voltages of more than 32V unless approved in writing by the instructor.
- Do not modify the wiring or attempt repair of any lab equipment.
- Most of the lab equipment operates from 120V AC, which is a lethal voltage. Never pull on a cord to unplug it as this can cause damage to the strain relief and insulation, potentially resulting in exposed electrical conductors.
- Please notify the TA, faculty member, or staff member and stop using the equipment immediately if you see nicks or damage to a power cord or other hazardous conditions.

Computers:

- Students should not install any software on the lab computers without approval of the TA, faculty member, or staff member.
- Students should not remove any of the cables on the computer and the monitor on the bench.
- In some labs, an HDMI cable is wired into each workstation for configuring Raspberry Pi and similar computer hardware. This cable should not be disconnected from the monitor.
- No device connected to the wired network of a lab should also have a WiFi connection enabled as this represents a security risk. This includes both personal student laptops and activating WiFi direct on printers.

Institution Information

UTA students are encouraged to review the below institutional policies and informational sections and reach out to the specific office with any questions. To view this institutional information, please visit the Institutional Information page (http://www.uta.edu/provost/administrative-forms/course-syllabus/index.php) which includes the following policies among others:

- Drop Policy
- Disability Accommodations
- Title IX Policy
- Academic Integrity
- Student Feedback Survey
- Final Exam Schedule

Additional Information

Face Covering Policy:
Face coverings are not mandatory; all students and instructional staff are welcome to wear face coverings while they are on campus or in the classroom.

Attendance:

At The University of Texas at Arlington, taking attendance is not required but attendance is a critical indicator of student success. Each faculty member is free to develop his or her own methods of evaluating students' academic performance, which includes establishing course-specific policies on attendance. However, while UT Arlington does not require instructors to take attendance in their courses, the U.S. Department of Education requires that the University have a mechanism in place to mark when Federal Student Aid recipients "begin attendance in a course." UT Arlington instructors will report when students begin attendance in a course as part of the final grading process. Specifically, when assigning a student a grade of F, faculty report must the last date a student attended their class based on evidence such as a test, participation in a class project or presentation, or an engagement online via Canvas. This date is reported to the Department of Education for federal financial aid recipients.

In this course, attendance in-class, on-campus is expected. Attending tests and laboratories in person is required.

Emergency Exit Procedures:
Should we experience an emergency event that requires evacuation of the building, students should exit the room and move toward the nearest exit. When exiting the building during an emergency, do not take an elevator but use the stairwells instead. Faculty members and instructional staff will assist students in selecting the safest route for evacuation and will make arrangements to assist individuals with disabilities.

Academic Success Center
The Academic Success Center (ASC) includes a variety of resources and services to help you maximize your learning and succeed as a student at the University of Texas at Arlington. ASC services include supplemental instruction, peer-led team learning, tutoring, mentoring and TRIO SSS. Academic Success Center services are provided at no additional cost to UTA students. For additional information visit: Academic Success Center. To request disability accommodations for tutoring, please complete this form.

Emergency Phone Numbers

In case of an on-campus emergency, call the UT Arlington Police Department at **817-272-3003** (non-campus phone), **2-3003** (campus phone). You may also dial 911. Non-emergency number 817-272-3381