CSE4356 System on Chip Design
CSE5356 System on Chip Design
EE5315 System on Chip Design
Fall 2020

Instructor Information

Instructor:
Bill Carroll, Ph. D.
Jason Losh, Ph.D.

Office Number:
ERB 521 (Carroll)
ERB 649 (Losh)

Office Telephone Number:
+1 817-272-3785 (CSE Department)

Email Address:
carroll@uta.edu
jlosh@uta.edu

Faculty Profile:
https://mentis.uta.edu/explore/profile/bill-carroll
https://mentis.uta.edu/explore/profile/jason-losh

Office Hours:
E-mail and virtual Q&A sessions in Teams.

Graders:
Grader contact information will be sent to the course listserv after assignments are made.

Course Information

Section Information:
001

Time and Place of Class Meetings:
Lectures: Carroll – Synchronous online in Teams (TTh 2:00 to 3:30 PM)
Losh -- Videos will be recorded on campus in Echo360 and available in Canvas on demand.
Live sessions will be held in Teams for office hours and interactive help sessions.
Tests: On campus, October 6, November 24, 2-3:20pm, Rooms ERB 124, 125, 126, and 127
Laboratory: Labs in ERB 126 and 127 can be used for testing of your project. Lab access is limited to times when labs for other courses are not meeting and lab utilization is less than 20%.

Description of Course Content:
Design of FPGA-based system on chip solutions, including processor subsystems, FPGA fabric, processor to FPGA bridges, and device drivers. Prerequisite: C or better in CSE 3442 or EE5314.

Student Learning Outcomes:
Upon successful completion of this course, students will have knowledge of:

- Knowledge of the architecture of FPGA-based SoC solutions

- Differences between soft- and hard-processor subsystems (HPS)
- Survey of common hard-processor subsystems
- Detailed knowledge of the DE1 SoC development board and environment
- Functional knowledge of the Quartus development platform
- Review of Verilog coding
- Development, coding, and testing of FPGA-only solutions
- Development, coding, and testing of HPS-only solutions
- Review of ARM advanced memory bus architectures (AMBA)
- Creating bridges from the processor to the FPGA fabric
- Using Linux /dev/mem for basic interfacing
- Writing Linux device drivers for FPGA access
- Developing SoC real-world applications

Class Web Page:
Carroll: Course materials, assignments, videos, etc will be posted on Canvas.
Losh: Additional files will be provided as needed on the course web site at http://ranger.uta.edu/~jlosh/.

Communication:
Carroll: My primary communication link is email carroll@uta.edu. Course materials will be on Canvas.
Losh: All class-wide communication by the instructor, including distribution of homework sets, will occur via the class listserv. Please sign up for the CSE4356-L listserv by sending an e-mail from your UTA e-mail account to listserv@listserv.uta.edu from your UTA e-mail account (no subject line needed) and the command SUBSCRIBE CSE4356-L as the message body. You will then receive an e-mail from the listserv server to which you must acknowledge to join the listserv with "OK" in an e-mail.

Canvas will only be used for Echo360 access.

Textbooks and Other Course Materials:
FPGA half of course:
Victor P. Nelson, Bill D. Carroll, H. Troy Nagle, and J. David Irwin, Digital Logic Circuit Analysis and Design, 2ed. New York: Pearson, 2021. Pearson eText, ISBN 9780135297070.

HPS/SoC half of course:
Extensive references, datasheets, application notes, and class notes will be provided on the course web site at http://ranger.uta.edu/~jlosh/.

Students will checkout a DE1-SoC board for the semester.
Students can optionally checkout a Analog Discovery 2 board with serial adapter for the semester.
Additionally, all students will use their TM4C123GXL evaluation kit board from CSE3442 or EE5314.

Major Assignments and Examinations:

Digital Labs:	Various lab assignments will be made during the semester.
Digital Test:	Tuesday, October 6
HPS/SoC Test:	Tuesday, November 24
Project:	Thursday, December 3

Technology Requirements:
Students will need a computer capable of accessing Canvas and watching the Echo360 lectures. The computer and OS must be capable of running Intel Quartis Prime. Up to 5 USB devices can be used for project development. At least 3 USB type-A ports are recommended, but it is possible to work with as few as 2 ports.

Grading Information

Grading:
- Grade scale: A (90-100), B (80-89), C (70-79), D (60-69), and F (0-59)

- Grade calculation: Digital Test (25%), Digital Labs (25%), HPS/SoC Test (25%), Project (25%)
- The instructor reserves the right to make reasonable changes in performance evaluation as needed.
- Any request for re-grading must be submitted to the Grader within one week of the completion of grading. If, after requesting a re-grade from the Grader and getting a response, you may refer the case to the instructor iif you think further action is needed.

Test:

- Test is open-book, open-notes, calculators allowed.
- No makeup will be provided for any test missed. Generally, you can request an incomplete in the course and makeup the missed test in the following semester.

Labs:

- Labs are individual assignments. Discussing lab topics is allowed, but the submissions must be unique. Sharing of code is not allowed.

Project:

- The projects will consist of limited hardware work, significant FGPA development, and firmware development and it is expected that it will take approximately 80 hours to complete.
- Projects teams will consist of 1 or 2 students. Discussing project topics is allowed, but the submissions must be unique to the team. Sharing of code is not allowed.
- Interim deadlines for the project will apply.

Course Schedule

- Syllabus overview, course objectives, course resource requirements (1 hr) [Carroll & Losh]
- Discussion of DE1-SoC kit and check out. (0.5 hrs) [Carroll & Losh]
- Review of combinational logic, Verilog, and Quartus. (1.5 hrs) [Carroll]
- Review of sequential logic, Verilog, and Quartus (3 hrs) [Carroll]
- Designing registers and register stacks (1.5 hrs) [Carroll]
- Designing FIFO buffers (1.5 hrs) [Carroll]
- Designing counters and frequency dividers (1.5 hrs) [Carroll]
- Designing clocks and timers (1.5 hrs) [Carroll]
- Using the Quartus Signal Tap Logic Analyzer (1.5 hrs) [Carroll]
- Designing fractional frequency dividers (1.5 hrs) [Carroll]
- Project work time (1.5 hrs) [Carroll]
- Digital Test (1.5 hrs) [Carroll]
- Lab demos (1.5 hrs) [Carroll & Losh]
- Project introduction, selection of teams (0.5 hrs) [Losh]
- Project-specific lecture (UART design) (1.5 hrs) [Losh]
- AMBA, AXI, and Avalon MM interface (1 hr) [Losh]
- Using the Quartus Platform Design (was Qsys) (1.5 hr) [Losh]
- Designing a memory-mapped register interface (1.5 hrs) [Losh]
- Case study: Designing a PWM peripheral (2 hrs) [Losh]
- Virtual memory interface (/dev/mem) (1 hr) [Losh]
- Virtual file system (/sys/class/*) kernel module design (1.5 hrs) [Losh]
- Higher-level kernel modules (1 hr) [Losh]
- Interrupts in Linux (1 hr) [Losh]
- Project-specific lectures (2.5 hrs) [Losh]
- HPS/SoC Test (1.5 hrs) [Losh]

The instructors reserve the right to make changes in the schedule as needed as the class progresses.

The official dates for registration, census, and dropping are available at www.uta.edu/acadcal.

Academic Integrity

This information is copied from http://www.uta.edu/conduct/academic-integrity/index.php.

The University of Texas at Arlington strives to uphold and support standards of personal honesty and integrity for all students consistent with the goals of a community of scholars and students seeking knowledge and responsibility. Furthermore, it is the policy of the University to enforce these standards through fair and objective procedures governing instances of alleged dishonesty, cheating, and other academic/non-academic misconduct.

Scholastic dishonesty includes, but is not limited to, cheating, plagiarism, and collusion on an examination or an assignment being offered for credit. Each student is accountable for work submitted for credit, including group projects.

- Cheating
  - Copying another's test or assignment (added note: remember this includes homework!)
  - Communication with another during an exam or assignment (i.e. written, oral or otherwise)
  - Giving or seeking aid from another when not permitted by the instructor
  - Possessing or using unauthorized materials during the test
  - Buying, using, stealing, transporting, or soliciting a test, draft of a test, or answer key
- Plagiarism
  - Using someone else's work in your assignment without appropriate acknowledgement
  - Making slight variations in the language and then failing to give credit to the source
- Collusion
  - Without authorization, collaborating with another when preparing an assignment

Safety Rules for ERB 124, 125, 126, and 127 Labs:

Scope:

- All UTA safety rules and regulations must be followed.
- These rules are in addition to UTA lab safety rules.
- In the event that a rule contained below is in conflict with UTA lab safety rules, the UTA safety rules shall supersede.

General rules:

- Students can only be in the lab when a graduate teaching assistant (GTA), faculty member, or staff member is present.
- Students should be professional at all times in the lab.
- Food and drinks are not allowed in the lab at any time.
- When leaving the lab, all work surfaces and floors should be clear of breadboards, cables, wires, and tools prior to leaving.
- When leaving the bench, turn off all lab equipment and unplug soldering irons.
- When leaving the bench, make sure that all cables, tools, and soldering equipment are properly stored in the correct location.
- Please ensure that the lab is kept in a neat and tidy manner.
- Please pick up any loose wires or parts on the bench and floor before leaving the lab. There is a push broom and dust pan in both rooms.
- Note any hazards observed in the lab to the GTA, faculty, or staff member immediately.
- For test equipment incorporating multi-language menus, such as oscilloscopes, please return the language to English before leaving the bench.
- When returning parts that are not consumables, make certain that the parts are returned to the correct drawer. If you are not certain, please leave them with the GTA, faculty member, or staff member.

- Students should store backpacks and similar items in a way that does not create a trip hazard to others.

Personal protective equipment (PPE):
- Safety glasses must be worn at all times when using the soldering irons or using cutting tools, such as diagonal cutters, in the lab.
- Face masks must be worn at all times in the lab.

Soldering irons:
- Soldering must be performed in the labs only at the soldering benches.
- Soldering irons should be used with care, while wearing safety glasses, and only after receiving training.
- When soldering and removing parts, or reworking a board, please use special care to ensure that solder is not splattered.
- Soldering irons must be placed back in their soldering station holder when not soldering to reduce the chance of injury or fire.
- Please keep the soldering station sponges wet when cleaning the iron tip but ensure that water is not spilled on the floor creating a slip hazard.
- Use the soldering iron smoke absorber fan units when soldering. Use them so that the exhaust air flow upwards.
- Some solders can contain lead, so wash hands thoroughly after using the soldering irons. No eating or drinking is allowed in the lab, as previously stated.
- No self-contained butane soldering irons are permitted.

Hand tools:
- Hand tools must be used with care and only when safety glasses are being worn.
- Diagonal cutters in particular can create tension on the wires during the cutting process, ejecting the loose wire, so please use special care.

Small powered rotary tools:
- Short use of powered cutting tools such as “Dremel” or small drill/driver can only be used at the soldering tables using a backup board to prevent damage to the tables.
- You must wear safety glasses.
- You must remove jewelry, necklaces, and lanyards and tie back long hair.
- For extended machining tasks, please use the designated Makerspace areas that are designed to handle the additional safety requirements and dust inhalation hazards instead.

Electrical hazards:
- The labs for these classes use voltages of 30V or less, but care must always be shown in using electrical circuits, regardless of the voltage.
- Do not use voltages of more than 30V unless approved in writing by the instructor.
- Do not modify the wiring or attempt repair of any lab equipment.
- Most of the lab equipment operates from 120V AC, which is a lethal voltage. Never pull on a cord to unplug it as this can cause damage to the strain relief and insulation,potentially resulting in exposed conductors.
- Please notify the GTA, faculty member, or staff member and stop using the equipment immediately if you see nicks or damage to a power cord.

Computers:
- Students should not install any software on the lab computers without approval of the GTA, faculty member, or staff member.
- Students should not remove any of the cables on the computer and the monitor on the bench.
- For external connection, an HDMI cable is provided at each workstation for configuring Raspberry Pi and similar computer hardware. This cable should not be disconnected from the monitor.

Institution Information

UTA students are encouraged to review the below institutional policies and informational sections and reach out to the specific office with any questions. To view this institutional information, please visit the Institutional Information page (http://www.uta.edu/provost/administrative-forms/course-syllabus/index.php) which includes the following policies among others:

- Drop Policy
- Disability Accommodations
- Title IX Policy
- Academic Integrity
- Student Feedback Survey
- Final Exam Schedule

Additional Information

Mandatory Face Covering Policy:
All students and instructional staff are required to wear facial coverings while they are on campus, inside buildings and classrooms. Students that fail to comply with the facial covering requirement will be asked to leave the class session. If students need masks, they may obtain them at the Central Library, the E.H. Hereford University Center's front desk or in their department. Students who refuse to wear a facial covering in class will be asked to leave the session by the instructor, and, if the student refuses to leave, they may be reported to UTA's Office of Student Conduct.

Attendance:
At The University of Texas at Arlington, taking attendance is not required but attendance is a critical indicator of student success. Each faculty member is free to develop his or her own methods of evaluating students' academic performance, which includes establishing course-specific policies on attendance. As the instructor of this section, However, while UT Arlington does not require instructors to take attendance in their courses, the U.S. Department of Education requires that the University have a mechanism in place to mark when Federal Student Aid recipients "begin attendance in a course." UT Arlington instructors will report when students begin attendance in a course as part of the final grading process. Specifically, when assigning a student a grade of F, faculty report must the last date a student attended their class based on evidence such as a test, participation in a class project or presentation, or an engagement online via Canvas. This date is reported to the Department of Education for federal financial aid recipients.

Emergency Exit Procedures:
Should we experience an emergency event that requires evacuation of the building, students should exit the room and move toward the nearest exit. When exiting the building during an emergency, do not take an elevator but use the stairwells instead. Faculty members and instructional staff will assist students in selecting the safest route for evacuation and will make arrangements to assist individuals with disabilities.

Student Success Programs:
UT Arlington provides a variety of resources and programs designed to help students develop academic skills, deal with personal situations, and better understand concepts and information related to their courses. Resources include tutoring by appointment, drop-in tutoring, etutoring, supplemental instruction, mentoring (time management, study skills, etc.), success coaching, TRIO Student Support Services, and student success workshops. For additional information, please email resources@uta.edu, or view the Maverick Resources website.

Emergency Phone Numbers

In case of an on-campus emergency, call the UT Arlington Police Department at **817-272-3003** (non-campus phone), **2-3003** (campus phone). You may also dial 911. Non-emergency number 817-272-3381