CSE4372/5372 RISC Processor Design CSE6351 Advanced Topics in Computer Engineering

Spring 2023

(subject to change prior to the first day of class, revised 1/10 and 1/16)

Instructor Information

Instructor: Jason Losh, Ph.D.

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Email Address:

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Faculty Profile:

https://mentis.uta.edu/explore/profile/jason-losh

Office Hours:

Office hours will be TTh 9:30-10:30am or by appointment for maximum flexibility.

Teaching Assistants:

Due to the requirement to post information related to the costs of a course at least 30 days before the beginning of classes, no TA information is available. The TA information will be given out during the first day of class and is not part of the syllabus.

Course Information

Section Information:

001

Time and Place of Class Meetings:

Lecture: TTh 5:30-6:50pm, ERB 129 This is a 100% face-to-face course. This is not an online course.

Description of Course Content:

Design of a RISC processor, based on RISC-V and custom instruction set architectures with implementation on an FPGA target for test and verification. Prerequisite: C or better in CSE 3442 or a passing grade in CSE 5400.

Student Learning Outcomes:

Upon successful completion of this course, students will have knowledge of:

- CPU Design: ALU, Registers, Memory Interface, Control Unit
- RISC-V Architecture and RV32IZmmul ISA
- On-chip and SDRAM Memory Access from FPGA
- Pipeline Design
- Data, Structural, and Control Hazards
- Stall/Forwarding Resolution
- RISC Implementation on FPGA

Class Web Page:

Additional files will be provided as needed on the course web site at http://ranger.uta.edu/~jlosh/.

Communication:

All class-wide communication by the instructor, including distribution of homework sets, will occur via the class listserv. If you are enrolled prior to the first day of class, you will be added to the listserv automatically. If you add on or after the first day of class, please sign up for the CSE4372-L listserv by sending an e-mail from your UTA e-mail account to <u>listserv@listserv.uta.edu</u> from your UTA e-mail account (no subject line needed) and the command SUBSCRIBE CSE4372-L as the message body. You will then receive an e-mail from the listserv server to which you must acknowledge to join the listserv with "OK" in an e-mail.

Canvas will only be used for Echo360 access.

Textbooks and Other Course Materials:

No textbook will be required for this course. Extensive references, datasheets, application notes, and class notes will be provided on the course web site.

Major Assignments and Examinations:

Test:	Tuesday, April 18
Project:	Friday, April 28
Labs:	6-8 labs will be assigned across the semester.

Technology Requirements:

The computer and OS must be capable of running GNU cross-compiler tools for the RISC-V. Ubuntu is used in the labs and lectures. Current computer recommendations are available at https://www.uta.edu/academics/schools-colleges/engineering/students/student-computer

Grading Information

Grading:

- Grade scale: A (90-100), B (80-89), C (70-79), D (60-69), and F (0-59)
- Grade calculation:
 - If TA support is sufficient:

Test (25%), Project (35%), Labs (40%)

- If TA support is not sufficient:
 - Project (50%), Labs (50%)
- Failure to submit all labs substantially complete will automatically result in a course grade of D or lower.
- The instructor reserves the right to make reasonable changes in performance evaluation as needed.
- The instructor also reserves the right to make substantial changes in the structure of the course if the modality of the course must be changed.
- Any request for re-grading must be submitted to the teaching assistant within one week of the completion of grading. If, after requesting a re-grade from the teaching assistant and getting a response, you may refer the case to the instructor if you think further action is needed.

Test:

- If TA support is not sufficient, there will be no test in the course.
- To ensure that all students are treated equally and given the same time to prepare for the exam, no makeup will be provided for any test missed.
- If you know you are going to miss a test, you can request an advance test given 1 week prior to the normally scheduled time for the exam, with the understanding that any curve applied to the test taken at the official test time will not apply to the advance test, since the content of that test will be unique.

- Test is on-campus
- Test is open-book, open-notes, calculators allowed.
- No makeup will be provided for any test missed. Generally, you can request an incomplete in the course and makeup the missed test in the following semester.

Labs:

• Labs are individual assignments. Discussing lab topics is allowed, but the submissions must be unique. Sharing of code is not allowed.

Project:

- Projects are individual assignments. Discussing project topics is allowed, but the submissions must be unique. Sharing of code is not allowed.
- Interim deadlines will occur as part of the lab exercises.

Course Schedule

- GNU cross-compiler toolchain, ELF files, Machine code extraction
- System Verilog examples
- RISC-V RV32IZmmul ISA
- RISC-V RV32I 5-stage Pipeline Design (IF/ID-RR/EX/M/WB)
- ALU design and RISC-V func3/func7/opcode to ALU control mapping
- RV32I compatible register file (parallel rs1 read, rs2 read, writeback)
- Inferring On-chip M9K memory (and common synthesis errors with async reads)
- Initializing memories with program data and constants with bit-streams
- PC counter design (linear code flow for now)
- I-memory and instruction word fetching
- Immediate sign-extension and control unit signals from instruction word
- Register read (no data forwarding from WB for now)
- ALU args solely from registers and immediates (no data forwarding from WB or EX for now) (no PC jump/branch calculations in ALU for now)
- ALU control from f3/7/op and ALU output
- Expanding ALU operation for address generation
- Expanding ALU for PC calculations
- Adding Zmmul and Zicsr support
- Data memory and support for 8-, 16-, and 32-bit signed and unsigned data r/w
- Register writeback from memory or ALU operation
- Data forward from WB stage to RR stage
- Data forward from WB stage and EX stage to EX stage
- Stall generation (when all else fails)
- Branch unit and branch argument forwarding from WB, M, and EX stages
- Flush logic

The instructor reserves the right to make changes in the schedule as needed as the class progresses.

The official dates for registration, census, and dropping are available at www.uta.edu/acadcal.

Academic Integrity

This information is extracted from http://www.uta.edu/conduct/academic-integrity/index.php.

The University of Texas at Arlington strives to uphold and support standards of personal honesty and integrity for all students consistent with the goals of a community of scholars and students seeking knowledge and responsibility. Furthermore, it is the policy of the University to enforce these standards through fair and objective procedures governing instances of alleged dishonesty, cheating, and other academic/non-academic misconduct.

Scholastic dishonesty includes, but is not limited to, cheating, plagiarism, and collusion on an examination or an assignment being offered for credit. Each student is accountable for work submitted for credit, including group projects.

- Cheating
 - Copying another's test or assignment (added note: remember this includes homework!)
 - Communication with another during an exam or assignment (i.e. written, oral or otherwise)
 - Giving or seeking aid from another when not permitted by the instructor
 - Possessing or using unauthorized materials during the test
 - o Buying, using, stealing, transporting, or soliciting a test, draft of a test, or answer key
- Plagiarism
 - Using someone else's work in your assignment without appropriate acknowledgement
 - Making slight variations in the language and then failing to give credit to the source
- Collusion
 - Without authorization, collaborating with another when preparing an assignment

Safety Rules for ERB 121-127 and 132 Labs:

Scope:

- All UTA safety rules and regulations must be followed.
- These rules are in addition to UTA lab safety rules.
- In the event that a rule contained below is in conflict with UTA lab safety rules, the UTA safety rules shall supersede.

General rules:

- Students can only be in the lab when a teaching assistant (TA), faculty member, or staff member is present.
- Students should be professional at all times in the lab.
- Food and drinks are not allowed in the lab at any time.
- When leaving the lab, all work surfaces and floors should be clear of breadboards, cables, wires, and tools prior to leaving.
- When leaving the bench, turn off all lab equipment and unplug soldering irons.
- When leaving the bench, make sure that all cables, tools, and soldering equipment are properly stored in the correct location.
- Please ensure that the lab is kept in a neat and tidy manner.
- Please pick up any loose wires or parts on the bench and floor before leaving the lab.
- Note any hazards observed in the lab to the TA, faculty, or staff member immediately.
- For test equipment incorporating multi-language menus, such as oscilloscopes, please return the language to English before leaving the bench.
- When returning parts that are not consumables, make certain that the parts are returned to the correct drawer. If you are not certain, please leave them with the TA, faculty member, or staff member.
- Students should store backpacks and similar items in a way that does not create a trip hazard to others.

Soldering irons:

• Soldering must be performed in the labs only at the soldering benches.

- Soldering irons should be used with care, while wearing safety glasses, and only after receiving training.
- When soldering and removing parts, or reworking a board, please use special care to ensure that solder is not splattered.
- Soldering irons must be placed back in their soldering station holder when not soldering to prevent the chance or injury or fire.
- Please keep the soldering station sponges wet when cleaning the iron tip but ensure that water is not spilled on the floor creating a slip hazard.
- Use the soldering iron smoke absorber fan units when soldering. Use them in the horizontal position to prevent directing air flow across the table into the face of another user.
- Some solders can contain lead, so wash hands thoroughly after using the soldering irons. No eating or drinking is allowed in the lab, as previously stated. The green solder spools in the lab generally indicate a lead-free solder.
- No self-contained butane soldering irons are permitted.
- Wear appropriate personal protection equipment (PPE).

Chemicals and lasers:

- In labs where chemicals or lasers are used, students must receive the appropriate safety training prior to working in the lab.
- In labs with chemicals, consult the safety data sheet (SDS) folder for information.
- Wear appropriate personal protection equipment (PPE) at all times.
- If transferring chemicals to secondary containers, clearly mark the contents of the container.

Hand tools:

- Hand tools must be used with care and only when safety glasses are being worn.
- Diagonal cutters in particular can create tension on the wires during the cutting process, ejecting the loose wire, so please use special care.
- Wear appropriate personal protection equipment (PPE).

Power tools:

- Short time use of small powered cutting tools such as a drill/driver can only be used at the soldering tables using a backup board to prevent damage to the tables.
- For extended machining tasks, please use the designated Makerspace areas that are designed to handle the additional safety requirements and dust inhalation hazards instead.
- Wear appropriate personal protection equipment (PPE).
- Jewelry, necklaces, and lanyards should be removed.
- Long hair should be tied back to prevent being caught in the tool.
- For labs with drill presses, band saws, laser cutters, CNC machines, and similar equipment, students must take the appropriate safety training prior to using the equipment.

Electrical hazards:

- The labs for these classes generally use voltages of 30V or less, but care must always be shown in using electrical circuits, regardless of the voltage.
- Do not use voltages of more than 30V unless approved in writing by the instructor.
- Do not modify the wiring or attempt repair of any lab equipment.
- Most of the lab equipment operates from 120V AC, which is a lethal voltage. Never pull on a cord to unplug it as this can cause damage to the strain relief and insulation, potentially resulting in exposed conductors.
- Please notify the TA, faculty member, or staff member and stop using the equipment immediately if you see nicks or damage to a power cord or another hazardous condition.

Computers:

- Students should not install any software on the lab computers without approval of the TA, faculty member, or staff member.
- Students should not remove any of the cables on the computer and the monitor on the bench.

• In some labs, an HDMI cable is provided at each workstation for configuring Raspberry Pi and similar computer hardware. This cable should not be disconnected from the monitor.

Institution Information

UTA students are encouraged to review the below institutional policies and informational sections and reach out to the specific office with any questions. To view this institutional information, please visit the <u>Institutional Information</u> page

(http://www.uta.edu/provost/administrative-forms/course-syllabus/index.php) which includes the following policies among others:

- Drop Policy
- Disability Accommodations
- Title IX Policy
- Academic Integrity
- Student Feedback Survey
- Final Exam Schedule

Additional Information

Face Covering Policy:

While face coverings are not mandatory, all students and instructional staff are welcome to wear face coverings while they are on campus or in the classroom.

Attendance:

At The University of Texas at Arlington, taking attendance is not required but attendance is a critical indicator of student success. Each faculty member is free to develop his or her own methods of evaluating students' academic performance, which includes establishing course-specific policies on attendance. However, while UT Arlington does not require instructors to take attendance in their courses, the U.S. Department of Education requires that the University have a mechanism in place to mark when Federal Student Aid recipients "begin attendance in a course." UT Arlington instructors will report when students begin attendance in a course as part of the final grading process. Specifically, when assigning a student a grade of F, faculty report must the last date a student attended their class based on evidence such as a test, participation in a class project or presentation, or an engagement online via Canvas. This date is reported to the Department of Education for federal financial aid recipients.

In this course, attendance in-class, on-campus is expected. Attending tests and laboratories in person is required.

Emergency Exit Procedures:

Should we experience an emergency event that requires evacuation of the building, students should exit the room and move toward the nearest exit. When exiting the building during an emergency, do not take an elevator but use the stairwells instead. Faculty members and instructional staff will assist students in selecting the safest route for evacuation and will make arrangements to assist individuals with disabilities.

Academic Success Center

The Academic Success Center (ASC) includes a variety of resources and services to help you maximize your learning and succeed as a student at the University of Texas at Arlington. ASC services include supplemental instruction, peer-led team learning, tutoring, mentoring and TRIO SSS. Academic Success Center services are provided at no additional cost to UTA students. For additional information visit: <u>Academic Success Center</u>. To request disability accommodations for tutoring, please complete this <u>form</u>.

Emergency Phone Numbers

In case of an on-campus emergency, call the UT Arlington Police Department at **817-272-3003** (non-campus phone), **2-3003** (campus phone). You may also dial 911. Non-emergency number 817-272-3381.