EE4312 Advanced Microprocessor Systems
EE5313 Microprocessor Systems
CSE4358/5358 Microprocessor Systems
Spring 2020

Instructor Information

Instructor:
Jason Losh, Ph.D.

Office Number:
ERB 649

Office Telephone Number:
+1 817-272-3785 (CSE Department)

Email Address:
jlosh@uta.edu

Faculty Profile:
https://mentis.uta.edu/explore/profile/jason-losh

Office Hours:
Monday 1:15-2:15pm, Wednesday 1:15-2:15pm, and by appointment. Additional hours will be added as needed as the semester proceeds.

Graders:
Grader contact information will be sent to the course listserv after assignments are made.

Course Information

Section Information:
001

Time and Place of Class Meetings:
Lecture: MW 4-5:20pm, SH 105

Description of Course Content:
Hardware/software development techniques for microprocessors with emphasis on asynchronous and synchronous memory interfaces, optimizing data throughput, and modern bus architectures. Topics include DMA controller design, SDRAM controller design, and real-world interfacing. Prerequisite: EE3310 or equivalent.

Student Learning Outcomes:
Upon successful completion of this course, students will have knowledge of:

- Knowledge of microprocessor and microcontroller architectures
- Proficiency in memory organization and interfacing (up to 64-bit widths), refresh, error correction (ECC)
- Application of EEPROM, flash, and RAM (SRAM, DRAM, FPM, EDO, SDRAM, DDRx)
- Analysis of data throughput with programmed i/o and DMA
- Design of SDRAM/DDRx memory controllers

- Use of software and hardware interrupts and interrupt service routines
- Understanding of tradeoffs between interrupts and polling (latency, effective rates, and efficiency)
- Introductory knowledge of coprocessor interfacing and multi-processor design
- Knowledge of multiple clock generation, phase locked loop, and handling asynchronous data
- Working knowledge of I/O buses and interfaces: ISA/PCI/PCIe, AMBA

Class Web Page:
Additional files will be provided as needed on the course web site at http://ranger.uta.edu/~jlosh/.

Communication:
All class-wide communication by the instructor, including distribution of homework sets, will occur via the class listserv. Please sign up for the EE5313-L listserv by sending an e-mail from your UTA e-mail account to listserv@listserv.uta.edu from your UTA e-mail account (no subject line needed) and the command SUBSCRIBE EE5313-L as the message body. You will then receive an e-mail from the listserv server to which you must acknowledge to join the listserv with "OK" in an e-mail.

Canvas will only be used for Echo360 access.

Textbooks and Other Course Materials:
No textbook will be required for this course. Extensive references, datasheets, application notes, and class notes will be provided on the course web site.

Major Assignments and Examinations:
Test 1: Monday, March 2
Test 2: Monday, April 27
Project: Monday, May 4

Grading Information

Grading:
- Grade scale: A (90-100), B (80-89), C (70-79), D (60-69), and F (0-59)
- Grade calculation: Test 1 (33.3%), Test 2 (33.3%), Project (33.3%)
- The instructor reserves the right to make reasonable changes in performance evaluation as needed.
- Any request for re-grading must be submitted to the Grader within one week of the completion of grading.

Tests:
- Tests are open-book, open-notes, calculators allowed.
- No makeup will be provided for any test missed.

Project:
- The project will consist of a paper-only design. It is expected that it will take approximately 60 hours to complete.
- Project teams will consist of one to three team members.

Course Schedule

- Introduction (0.5 hour)
- Review of Digital Logic and Symbols Used in Class (0.5 hour)
- Computer Architecture Basics (2 hrs)
- Memory Interfacing Overview (0.5 hour)
- Memory Maps and Decoders (0.5 hour)

- Processor Subsystem Design:
  Clocking (synchronizing), control buses, address latching (1.5 hours)
- Banks and basic RO memory interfacing (1.5 hours)
- Timing analysis (1.5 hours)
- Asynchronous RAM interfacing (1,5 hours)
- Wait state generation, synchronizing ready signal (0.5 hour)
- C program memory access and bank usage correlation (0.5 hour)
- DRAM theory of operation, refresh controller design (2.5 hours)
- Fast page mode memory (1 hour)
- Synchronous memory introduction, timing cycles (1.5 hours)
- Exam 1 (1.5 hrs)
- SDRAM/DDRx controller design (1 hour)
- DMA controller design (6 hours)
- Interrupt controller design, study of NVIC/GIC (1.5 hours)
- System design of high speed analog capture/generation device using interrupts, DMA, memory (3.5 hours)
- Introduction to cache design (3 hours)
- Project support lecture content (7 hrs)
- Exam 2 (1.5 hrs)

The instructor reserves the right to make changes in the schedule as needed as the class progresses.

The official dates for registration, census, and dropping are available at www.uta.edu/acadcal.

Academic Integrity

This information is copied from http://www.uta.edu/conduct/academic-integrity/index.php.

The University of Texas at Arlington strives to uphold and support standards of personal honesty and integrity for all students consistent with the goals of a community of scholars and students seeking knowledge and responsibility. Furthermore, it is the policy of the University to enforce these standards through fair and objective procedures governing instances of alleged dishonesty, cheating, and other academic/non-academic misconduct.

Scholastic dishonesty includes, but is not limited to, cheating, plagiarism, and collusion on an examination or an assignment being offered for credit. Each student is accountable for work submitted for credit, including group projects.

- Cheating
  - Copying another's test or assignment (added note: remember this includes homework!)
  - Communication with another during an exam or assignment (i.e. written, oral or otherwise)
  - Giving or seeking aid from another when not permitted by the instructor
  - Possessing or using unauthorized materials during the test
  - Buying, using, stealing, transporting, or soliciting a test, draft of a test, or answer key
- Plagiarism
  - Using someone else's work in your assignment without appropriate acknowledgement
  - Making slight variations in the language and then failing to give credit to the source
- Collusion
  - Without authorization, collaborating with another when preparing an assignment

Institution Information

UTA students are encouraged to review the below institutional policies and informational sections and reach out to the specific office with any questions. To view this institutional information, please visit the Institutional Information page (http://www.uta.edu/provost/administrative-forms/course-syllabus/index.php) which includes the following policies among others:

- Drop Policy
- Disability Accommodations
- Title IX Policy
- Academic Integrity
- Student Feedback Survey
- Final Exam Schedule

Additional Information

Attendance:
At The University of Texas at Arlington, taking attendance is not required but attendance is a critical indicator of student success. Each faculty member is free to develop his or her own methods of evaluating students' academic performance, which includes establishing course-specific policies on attendance. As the instructor of this section, However, while UT Arlington does not require instructors to take attendance in their courses, the U.S. Department of Education requires that the University have a mechanism in place to mark when Federal Student Aid recipients "begin attendance in a course." UT Arlington instructors will report when students begin attendance in a course as part of the final grading process. Specifically, when assigning a student a grade of F, faculty report must the last date a student attended their class based on evidence such as a test, participation in a class project or presentation, or an engagement online via Canvas. This date is reported to the Department of Education for federal financial aid recipients.

Emergency Exit Procedures:
Should we experience an emergency event that requires evacuation of the building, students should exit the room and move toward the nearest exit. When exiting the building during an emergency, do not take an elevator but use the stairwells instead. Faculty members and instructional staff will assist students in selecting the safest route for evacuation and will make arrangements to assist individuals with disabilities.

Student Success Programs:
UT Arlington provides a variety of resources and programs designed to help students develop academic skills, deal with personal situations, and better understand concepts and information related to their courses. Resources include tutoring by appointment, drop-in tutoring, etutoring, supplemental instruction, mentoring (time management, study skills, etc.), success coaching, TRIO Student Support Services, and student success workshops. For additional information, please email resources@uta.edu, or view the Maverick Resources website.

Emergency Phone Numbers

In case of an on-campus emergency, call the UT Arlington Police Department at **817-272-3003** (non-campus phone), **2-3003** (campus phone). You may also dial 911. Non-emergency number 817-272-3381