EE 5313 Microprocessor Systems
Fall 2003
MW 4:00-5:20pm, 109 NH

Instructor:
Jason Losh, Ph.D.
jlosh@uta.edu
Office Hours are before 4pm in 109NH, after 6:50pm in 148 NH, or in 509 NH by appointment.
E-mail is the quickest method of contacting me on non-class days.

Textbook:
The Intel Microprocessors – Architecture. Programming, and Interfacing by Brey, 2002, ISBN 0-13-060714-2

Catalog Description (Fall 2003 online version):
5313. MICROPROCESSOR SYSTEMS (3-0). Hardware/software development techniques for microprocessors and their programmable peripherals, with emphasis on multi-byte width memory design, throughput issues including DMA controller design, coprocessor operation, interrupt-driven i/o, oscillator issues and timer peripherals, analog signal interfacing, and digital buses and interfaces. Topics include: code efficiency issues, hardware-software interactions, and design of memory systems, DMA controllers, and real-world interfacing.

Prerequisites:
Familiarity with the 8086 processor or a very good knowledge of other processors, such as the 8088 or 68000, or microcontrollers, such as the HC11 or 8051, is important. Essential background includes assembly language programming, 8086 maximum-mode architecture, memory organization and timing, basic interfacing, and interrupt operation. Also, knowledge of C or C++ is important.

Course Topics:
- Course introduction and discussion of course objectives
- Survey of microprocessor and microcontroller architectures
- Review of 8086 assembly language programming and high-level language function calls
- Review of 8086 maximum-mode architecture, interfacing, timing, and memory
- Memory: organization and interfacing (up to 64-bit widths), refresh, and error correction (ECC), ROM (EPROM and flash) and RAM (SRAM, DRAM, FPM, EDO, SDRAM, time permitting: DDR and RDRAM)
- Data throughput issues: microprocessor block transfers and DMA
- Interrupts: software and hardware interrupts, interrupt service routines, and interrupt hooking
- Interrupts v. polling: latency, effective rates, and efficiency
- Coprocessors: FP and MMX (time permitting) interfacing and programming
- Clock issues: timers, interface reference clocks, sampling clocks, and asynchronizing blocks
- I/O issues: digital and analog signal interfacing, isolation, ground loops, noise, and EMI
- I/O buses and interfaces: PCI, ISA, RS-232/422/423/485, IEEE-1284, and IEEE-1394, and USB
- Miscellaneous controllers: video and magnetic media (as time permits)

Additional References:
Many resources will be provided in addition to the textbook. These documents will be posted at http://omega.uta.edu/~jlosh/.

Digital resources:
- *Digital Logic Design Principles* by Balabanian and Carlson, 2001, ISBN 0-471-29351-2
- *An Engineering Approach to Digital Design* by Fletcher, 1980, ISBN 0-13-277699-5

80x86 software resources:
- *The Art of Assembly Language Programming* by Hyde, http://cs.smith.edu/~thiebaut/ArtOfAssembly/artofasm.html
- *Intel Architecture Software Developer's Manual, vols. 1 through 3*, Intel 1999
- *The Programmer's PC Sourcebook* by Hogan, 1988, ISBN 1-55615-118-7

80x86 hardware resources:
- *Intel 386™ DX Microprocessor Datasheet*, Intel, 1995

- *Intel Pentium® Processor with MMX Technology*, Intel, 1997
- *Intel Pentium 4® Processor with 512-KB L2 Cache*, Intel, 2002
- *Microprocessors vols. 1 and 2*, Intel, 1992, ISBN 1-55512-150-0
- *Microprocessors and Interfacing – Programming and Hardware*, 2nd ed. by Hall, 1992, ISBN 0-07-025742-6
- *The 8088 and 8086 Microprocessors – Programming, Interfacing, Software, Hardware, and Applications, 3rd ed.* by Triebel and Singh, ISBN 0-13-010560-0
- *Microprocessor Systems: The 8086/8088 Family*, 2nd ed. by Liu and Gibson, 1986, ISBN 0-13-580499-X

Other microprocessor resources:
- *PowerPC™ Microprocessor Family: The Bus Interface for 32-bit Microprocessors*, Motorola, 1997
- *PowerPC 603e™ RISC Microprocessor Family PID7t-603e Specification*, TSPC603R, Atmel, 2002

Important Dates:
First Day of Classes (Monday, 8/25), Labor Day Holiday (Monday, 9/1), Census Date (Wednesday, 9/10), Test 1 (Monday, 9/29), Test 2 (Monday, 11/3), Last Day to Drop or Withdraw (Friday, 11/14), Project Due (Wednesday, 12/3 at 4pm), Test 3 (Wednesday, 12/10 from 2 to 4:30pm), Grades Due (Tuesday, 12/16), and Grades Available (Wednesday, 12/17).

Performance Assessment:
- Grade scale: A (90-100), B (75-89), C (60-74), D (50-59), and F (0-49)
- Grade calculation: (Test1 + Test2 + Test3 + Project) / 4
- The instructor reserves the right to make reasonable changes in performance evaluation as needed.

Graders:
Sankalp Mehrota, sankalpm4@hotmail.com
Paul Kim, paul72kim@hotmail.com
Indira Motamarri, indiraatuta@yahoo.com

Grader Hours in Rm 148NH:

M	Paul	2-4pm
	Indira	7-9pm
T	Sankalp	2-5pm
W	Indira	7-9pm
Th	Sankalp	5-8pm
S	Indira	10-12n
	Paul	12n-4pm

Tests (75% of Grade):
- Calculators, rulers, pencils, pens, books, and notes will be allowed during tests.
- Any device capable of compiling or emulating any 80x86 code can not be used during in-class portions of the tests.
- Take home portions of tests will be due within one week of assignment.
- No makeup will be provided for any test.
- Any request for re-grading must be submitted to the grader within one week of the return date.
- All students (on campus and off campus) shall take exams at the University of Texas at Arlington.
- For all tests, Web students shall take exams at the same time as on-campus students.
- For Tests 1 and 2, VCR students may take tests during the normal scheduled class time or up to one week later.
- For Test 3, VCR students shall take the exam at the same time as on-campus students. To be fair to VCR students in this regard, the last two dates of class will not be on the exam, to allow proper time for review.

Project (25% of Grade):
- Project teams will consist of one to three team members.
- The project is due at the beginning of the final day of class, which is Wednesday, 12/3.
- Off campus (VCR and Web) students shall also meet this deadline for the project.

Academic Honesty:
It is the philosophy of The University of Texas at Arlington that academic dishonesty is a completely unacceptable mode of conduct and will not be tolerated in any form. All persons involved in academic

dishonesty will be disciplined in accordance with University regulations and procedures. Discipline may include suspension or expulsion from the University. “Scholastic dishonesty includes but is not limited to cheating, plagiarism, collusion, the submission for credit of any work or materials that are attributable in whole or in part to another person, taking an examination for another person, any act designed to give unfair advantage to a student or the attempt to commit such acts.” (Regents’ Rules and Regulations, Part One, Chapter VI, Section 3, Subsection 3.2, Subdivision 3.22). ANY CHEATING WILL RESULT IN SEVERE PENALTIES. All work submitted must be original. If derived from another source, a full bibliographical citation must be given.

Americans with Disabilities Act:
If you require an accommodation based on disability, please feel free to meet with me during the first week of the semester to make sure that you are properly accommodated. Contact Dr. Cheryl Cardell (272-3670) or Mr. Jim Hayes (272-3364) for more information.