EE 5315 DSP Processors
Fall 2007
5:30-6:50pm MW, 109 NH

Instructor:
Jason Losh, Ph.D.
jlosh@uta.edu
Office Hours are after 6:50pm MW outside the class room
E-mail is the quickest method of contacting me on non-class days.

Textbook:
Real-Time Digital Signal Processing: Implementations and Applications, 2nd ed., Sen M. Kuo, Bob H. Lee, Wenshun Tian, John Wiley & Sons, Inc., ISBN 0-470-01495-4, 2006.

Extensive references, datasheets, application notes, and class notes will be provided on the course web site at http://omega.uta.edu/~jlosh/.

Listserv:
Please sign up for the EE5315-L listserv to receive the latest updates (goto http://listserv.uta.edu to manage your subscriptions or send a message to listserv@listserv.uta.edu with no subject line and the command SUBSCRIBE EE5315-L as the message body).

Catalog Description:
5315. DSP MICROPROCESSORS (3-0). Device architectures and various aspects of hardware/software design will be presented for dominant families of function specific, application-specific, and general-purpose digital signal processors (DSPs) from leading manufacturers. Special attention will be given to problems related to real-time acquisition and processing of analog data (audio, video, RF, etc.), including design principles for the state-of-the-art data conversion interfaces. Prerequisite: EE 5313 or consent of instructor.

Prerequisite Background:
EE 5313 or passing grade on the leveling exam offered on the first day of class.

Very good knowledge of at least one microprocessor or microcontroller is mandatory. Essential background includes assembly language programming, memory organization, memory mapping, bus timing, DMA operation, and interrupts.

An understanding of digital filtering will also be very useful, but not required. Knowledge of Fourier series expansion, Fourier transform, and z-transform are required.

Course Topics:
- Course introduction and discussion of course objectives
- Study of basic microprocessor features including von Neuman v. Harvard memory architecture, pipelined v. non-pipelined instruction processing, parallelism, and ALU design
- Detailed study of the TMS320VC5509A digital signal processor including address-, data-, and program-flow units, pipelining, general purpose ALU and dual 17x17 bit multiplier/accumulators, 6 data buses, address generation, memory interfaces, internal dual- and single-access RAM, and standard ROM
- Detailed study of the TMS320VC5509A digital signal processor including address-, data-, and program-flow units, pipelining, general purpose ALU + dual 17x17 bit multipliers, 6 data buses, address generation, memory interfaces, internal dual- and single-access RAM and standard ROM
- Detailed study of the TMS320VC5509A peripherals including DMA controller, external memory interface, multichannel buffered serial ports, and GPIO
- Interfacing SDRAM, Flash, memory-mapped peripherals, and I/O-mapped peripherals

- Introduction to the Code Composer Studio environment and the 5509A DSK
- Working in a mixed C/ASM environment
- Study of addressing modes and the mnemonic instruction set
- Assembly coding with emphasis on writing efficient code callable from the C high-level language
- Development of real-time data processing applications

Important Dates:
First Class (Monday, 8/27), Labor Day Holiday (Monday, 9/3), Census Date (Wednesday, 9/13), Test 1 (Monday, 10/8), Last Drop Date (Friday, 11/2), Test 2 (Monday, 11/19), Project Due (Monday, 12/3 at 5:30pm)

Performance Assessment:
- Grade scale: A (90-100), B (75-89), C (60-74), D (50-59), and F (0-49)
- Grade calculation: (Test 1 + Test 2 + Project) / 3
- The instructor reserves the right to make reasonable changes in performance evaluation as needed.

Graduate Teaching Assistants:

Name	Email	Office Hours
Brijesh Chauhan	brijesh.chauhan@uta.edu	M 7-10 | W 7-10 | F10-2
Vijay Sankar	mr.vijaysankar@gmail.com	MW 7-10 | TTh 1-3:30
Venkata Praveen Goru	vgoru@uta.edu	MW 2:30-4 | T 6:30-9 | Th 6:30-8 | F 5-9
Gaurav Nasit	nasitgaurav@gmail.com	MW 1-2:30 & 4-7 | T 9-10 | Th 8-10

Tests:
- Calculators, rulers, pencils, pens, books, and notes will be allowed during tests.
- Any device capable of compiling or emulating microcontrollers or microprocessors can not be used during in-class portions of the tests.
- No makeup will be provided for any test.
- Any request for re-grading must be submitted to the grader within one week of the return date.
- Off campus students shall take exams on the same day as on-campus students.

Hardware Platform:
- The project will use the TMS320VC5509A DSK board from Spectrum Digital
- Enrollment is limited to guarantee that teams of 3 will receive a 5509A development kit (DSK) to check out for the semester.
- If adequate numbers of DSKs are available, teams of 1 and 2 members will be permitted.

Projects:
- Project teams will consist of three team members, with allowances for teams of 1 and 2 as possible
- Off campus students will be given first priority for forming smaller teams, since their geographic separation presents unique problems in some cases
- Project is due at the beginning of the class on Monday, 12/3.
- Off campus students shall also meet this deadline for the project.

Academic Integrity:
It is the philosophy of The University of Texas at Arlington that academic dishonesty is a completely unacceptable mode of conduct and will not be tolerated in any form. All persons involved in academic dishonesty will be disciplined in accordance with University regulations and procedures. Discipline may include suspension or expulsion from the University.

"Scholastic dishonesty includes but is not limited to cheating, plagiarism, collusion, the submission for credit of any work or materials that are attributable in whole or in part to another person, taking an

examination for another person, any act designed to give unfair advantage to a student or the attempt to commit such acts." (Regents' Rules and Regulations, Series 50101, Section 2.2)

EE Department Policy requires that you sign and return a letter acknowledging the College of Engineering Ethics policy.

Americans with Disabilities Act:
The University of Texas at Arlington is on record as being committed to both the spirit and letter of federal equal opportunity legislation; reference Public Law 92-112 - The Rehabilitation Act of 1973 as amended. With the passage of federal legislation entitled Americans with Disabilities Act (ADA), pursuant to section 504 of the Rehabilitation Act, there is renewed focus on providing this population with the same opportunities enjoyed by all citizens.

As a faculty member, I am required by law to provide "reasonable accommodations" to students with disabilities, so as not to discriminate on the basis of that disability. Student responsibility primarily rests with informing faculty of their need for accommodation and in providing authorized documentation through designated administrative channels. Information regarding specific diagnostic criteria and policies for obtaining academic accommodations can be found at www.uta.edu/disability. Also, you may visit the Office for Students with Disabilities in room 102 of University Hall or call them at (817) 272-3364.

Student Support Services:
The University of Texas at Arlington supports a variety of student success programs to help you connect with the University and achieve academic success. These programs include learning assistance, developmental education, advising and mentoring, admission and transition, and federally funded programs. Students requiring assistance academically, personally, or socially should contact the Office of Student Success Programs at 817-272-6107 for more information and appropriate referrals.