

EE6313 Advanced Microprocessor Systems

Fall 2019

Instructor Information

Instructor:

Jason Losh, Ph.D.

Office Number:

ERB 649

Office Telephone Number:

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Faculty Profile:

<https://mentis.uta.edu/explore/profile/jason-losh>

Office Hours:

Monday 10-10:50am, Tuesday 5-5:20pm, Thursday 12-12:30pm., Thursday 5-5:20pm, and by appointment. Additional hours will be added as needed as the semester proceeds.

Graders:

Grader contact information will be sent to the course listserv after assignments are made.

Course Information

Section Information:

001

Time and Place of Class Meetings:

Lecture: MW 2:30-3:50pm, WH 221

Description of Course Content:

Study of the advanced microprocessor architectures including 32/64-bit RISC and CISC families of microprocessors will be compared based on detailed architectural analysis of the selected devices. Topics include: address/instruction pipelines, burst cycles, memory caching and cache coherency issues, register renaming, speculative instruction execution and other performance-oriented techniques. Prerequisite: EE5313 or EE4312.

Student Learning Outcomes:

Upon successful completion of this course, students will have knowledge of:

- CPU Design: ALU, Registers, Memory Interface, Control Unit
- Instruction Set Attributes: Minimalism, Orthogonality, RISC/CISC
- Predication, Speculative Execution, and Out of Order Execution
- Protected Operating System Basics
- Privileged v. Unprivileged Operation
- Multitasking Operating Systems
- Pipelining: Design, Hazards, Stall/Forwarding Resolution
- Parallelism and Superscalar Architectures

- Cache Memory Design: Mapping, Miss/Hit, Replacement, Write-back Strategies
- Virtual Memory: Paging, Segmentation, Translation and Look-aside Buffers
- High-speed I/O Design, Modern Protocols: PCIe, SATA

Class Web Page:

Additional files will be provided as needed on the course web site at <http://omega.uta.edu/~jlosh/>.

Communication:

All class-wide communication by the instructor, including distribution of homework sets, will occur via the class listserv. Please sign up for the EE6313-L listserv by sending an e-mail from your UTA e-mail account to listserv@listserv.uta.edu from your UTA e-mail account (no subject line needed) and the command SUBSCRIBE EE6313-L as the message body. You will then receive an e-mail from the listserv server to which you must acknowledge to join the listserv with "OK" in an e-mail.

Canvas will only be used for Echo360 access.

Textbooks and Other Course Materials:

No textbook will be required for this course. Extensive references, datasheets, application notes, and class notes will be provided on the course web site at <http://omega.uta.edu/~jlosh/>.

Major Assignments and Examinations:

Project 1: Monday, October 21
Project 2: Monday, December 2

Grading Information

Grading:

- Grade scale: A (90-100), B (80-89), C (70-79), D (60-69), and F (0-59)
- Grade calculation: Project 1 (50%), Project 2 (50%)
- The instructor reserves the right to make reasonable changes in performance evaluation as needed.

Project:

- The project will consist of hardware construction and firmware development and it is expected that it will take approximately 80 hours to complete.
- Projects teams will consist of 1 or 2 students only. Work should not be shared between teams.

Course Schedule

- Differences between Harvard and von Neuman architectures (0.5 hrs)
- Differences of microcontroller and microprocessor architectures (0.5 hrs)
- Comparison of standard microprocessor and digital signal processor memory bus and ALU architectures (0.5 hrs)
- ALU design, ALU-register interface in load-store architectures (1.5 hrs)
- Fetching and control logic (3 hrs)
- Instruction set design as a function of selected architecture (1 hr)
- Instruction encoding (1 hr)
- Register-memory interface (1 hr)
- Complete 4-stage pipeline design (5 hrs)
- Hazards and techniques to mitigate: stalling, data forwarding, speculation (2 hrs)
- Predication, Speculative Execution, and Out of Order Execution (1.5 hrs)
- Superscalar and VLIW (1.5 hrs)
- Instruction-level parallelism (1 hr)
- Thread-level parallelism, multiprocessor, multicore designs (3 hrs)

- Multitasking Operating Systems (2 hrs)
- Security aspects, protected operating systems, concept of privilege (1.5 hrs)
- Virtualization of memory and paging (2 hrs)
- Cache controller design (6 hrs)
- High-speed I/O busses and design issues (1.5 hrs)

The instructor reserves the right to make changes in the schedule as needed as the class progresses.

The official dates for registration, census, and dropping are available at www.uta.edu/acadcal.

Academic Integrity

This information is copied from <http://www.uta.edu/conduct/academic-integrity/index.php>.

The University of Texas at Arlington strives to uphold and support standards of personal honesty and integrity for all students consistent with the goals of a community of scholars and students seeking knowledge and responsibility. Furthermore, it is the policy of the University to enforce these standards through fair and objective procedures governing instances of alleged dishonesty, cheating, and other academic/non-academic misconduct.

Scholastic dishonesty includes, but is not limited to, cheating, plagiarism, and collusion on an examination or an assignment being offered for credit. Each student is accountable for work submitted for credit, including group projects.

- Cheating
 - Copying another's test or assignment (added note: remember this includes homework!)
 - Communication with another during an exam or assignment (i.e. written, oral or otherwise)
 - Giving or seeking aid from another when not permitted by the instructor
 - Possessing or using unauthorized materials during the test
 - Buying, using, stealing, transporting, or soliciting a test, draft of a test, or answer key
- Plagiarism
 - Using someone else's work in your assignment without appropriate acknowledgement
 - Making slight variations in the language and then failing to give credit to the source
- Collusion
 - Without authorization, collaborating with another when preparing an assignment

Institution Information

UTA students are encouraged to review the below institutional policies and informational sections and reach out to the specific office with any questions. To view this institutional information, please visit the [Institutional Information](http://www.uta.edu/provost/administrative-forms/course-syllabus/index.php) page

(<http://www.uta.edu/provost/administrative-forms/course-syllabus/index.php>) which includes the following policies among others:

- Drop Policy
- Disability Accommodations
- Title IX Policy
- Academic Integrity
- Student Feedback Survey
- Final Exam Schedule

Additional Information

Attendance:

At The University of Texas at Arlington, taking attendance is not required but attendance is a critical indicator of student success. Each faculty member is free to develop his or her own methods of evaluating students' academic performance, which includes establishing course-specific policies on attendance. As the instructor of this section, However, while UT Arlington does not require instructors to take attendance in their courses, the U.S. Department of Education requires that the University have a mechanism in place to mark when Federal Student Aid recipients "begin attendance in a course." UT Arlington instructors will report when students begin attendance in a course as part of the final grading process. Specifically, when assigning a student a grade of F, faculty report must the last date a student attended their class based on evidence such as a test, participation in a class project or presentation, or an engagement online via Canvas. This date is reported to the Department of Education for federal financial aid recipients.

Emergency Exit Procedures:

Should we experience an emergency event that requires evacuation of the building, students should exit the room and move toward the nearest exit. When exiting the building during an emergency, do not take an elevator but use the stairwells instead. Faculty members and instructional staff will assist students in selecting the safest route for evacuation and will make arrangements to assist individuals with disabilities.

Student Success Programs:

UT Arlington provides a variety of resources and programs designed to help students develop academic skills, deal with personal situations, and better understand concepts and information related to their courses. Resources include [tutoring by appointment](#), [drop-in tutoring](#), [etutoring](#), [supplemental instruction](#), [mentoring](#) (time management, study skills, etc.), [success coaching](#), [TRIO Student Support Services](#), and [student success workshops](#). For additional information, please email resources@uta.edu, or view the [Maverick Resources](#) website.

Emergency Phone Numbers

In case of an on-campus emergency, call the UT Arlington Police Department at **817-272-3003** (non-campus phone), **2-3003** (campus phone). You may also dial 911. Non-emergency number 817-272-3381