

Device Operation

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Note : All descriptions are described based on following conditions.

Burst Length=4, Cas Latency=2,
tRCD=3clk, tRP=3clk, tCCD=1clk, tDQSS=1clk, tDPL=1clk, tDRL=1clk

POWER-UP SEQUENCE AND DEVICE INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to VDD, then to VDDQ, and finally to VREF (and to the system VTT). VTT must be applied after VDDQ to avoid device latch-up, which may cause permanent damage to the device. VREF can be applied anytime after VDDQ, but is expected to be nominally coincident with VTT. Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied. Maintaining an LVCMOS LOW level on CKE during power-up is required to guarantee that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200us delay prior to applying an executable command.

Once the 200us delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a EXTENDED MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any command. During the 200 cycles of CK, for DLL locking, executable commands are disallowed (a DESELECT or NOP command must be applied). After the 200 clock cycles, a PRECHARGE ALL command should be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

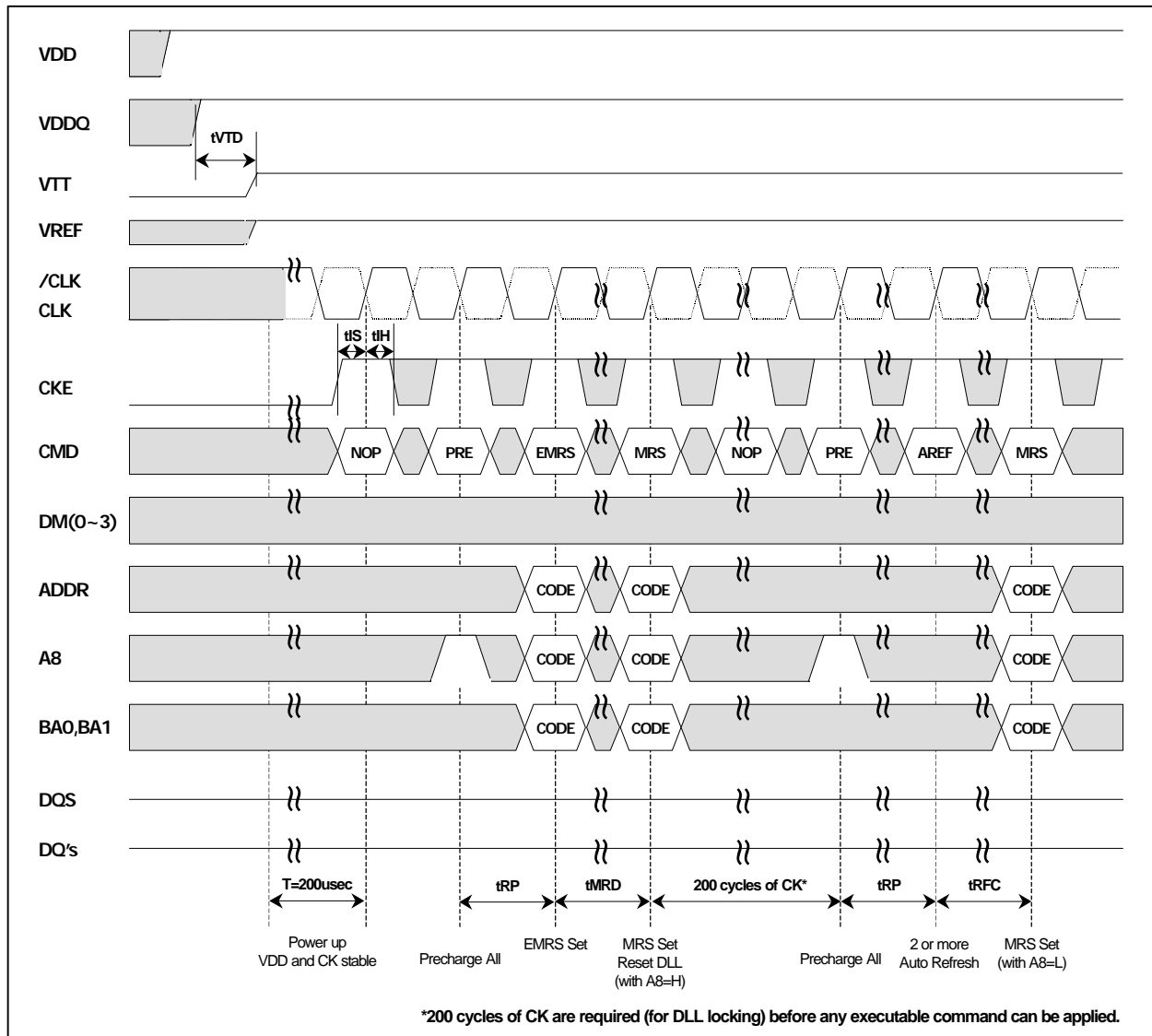
1. Apply power - VDD, VDDQ, VTT, VREF in the following power up sequencing and attempt to maintain CKE at LVC-MOS low state. (All the other input pins may be undefined.)
 - VDD and VDDQ are driven from a single power converter output.
 - VTT is limited to $1.44V$ (reflecting $VDDQ(max)/2 + 50mV$ VREF variation + $40mV$ VTT variation).
 - VREF tracks $VDDQ/2$.
 - A minimum resistance of 42 Ohms (22 ohm series resistor + 22 ohm parallel resistor - 5% tolerance) limits the input current from the VTT supply into any pin.
 - If the above criteria cannot be met by the system design, then the following sequencing and voltage relationship must be adhered to during power up.

Voltage description	Sequencing	Voltage relationship to avoid latch-up
VDDQ	After or with VDD	$< VDD + 0.3V$
VTT	After or with VDDQ	$< VDDQ + 0.3V$
VREF	After or with VDDQ	$< VDDQ + 0.3V$

2. Start clock and maintain stable clock for a minimum of 200usec.
3. After stable power and clock, apply NOP condition and take CKE high.
4. Issue Extended Mode Register Set (EMRS) to enable DLL.
5. Issue Mode Register Set (MRS) to reset DLL and set device to idle state with bit A8=High. (An additional 200 cycles of clock are required for locking DLL)
6. Issue Precharge commands for all banks of the device.

1. Issue 2 or more Auto Refresh commands.
2. Issue a Mode Register Set command to initialize the mode register with bit A8 = Low.

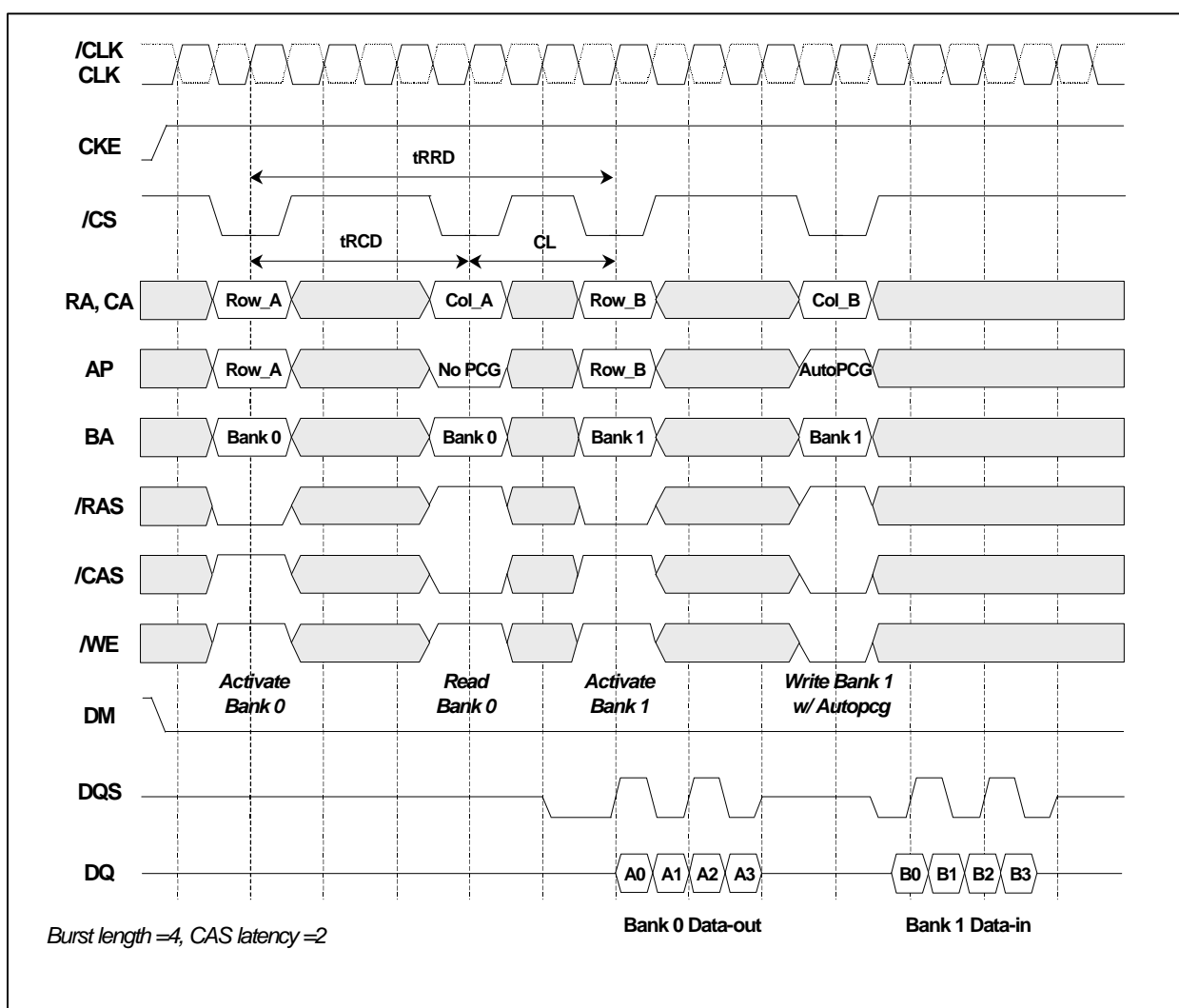
Power-Up Sequence



Burst Read and Burst Write

Burst Read and Burst Write commands are initiated as listed in Fig.1. Before the Burst Read command, the bank must be activated earlier. After /RAS to /CAS delay (t_{RCD}), read operation starts. DDR SDRAM has been implemented with Data Strobe signal (DQS) which toggles high and low during burst with the same frequency as clock (CLK, /CLK). After CAS Latency (CL) which is defined as the interval between command clock and the first rising edge of the DQS, read data is launched onto data pin (DQ) with reference to DQS signal edge. Burst Write command in another bank can be given with having activated that bank where /RAS to /RAS delay (t_{RRD}) is satisfied. Write data is also referenced and aligned to the DQS signal sent from the memory controller. Since all read operation bursts data out at both the rising and the falling of the DQS, double data bandwidth can be achieved, also for write data.

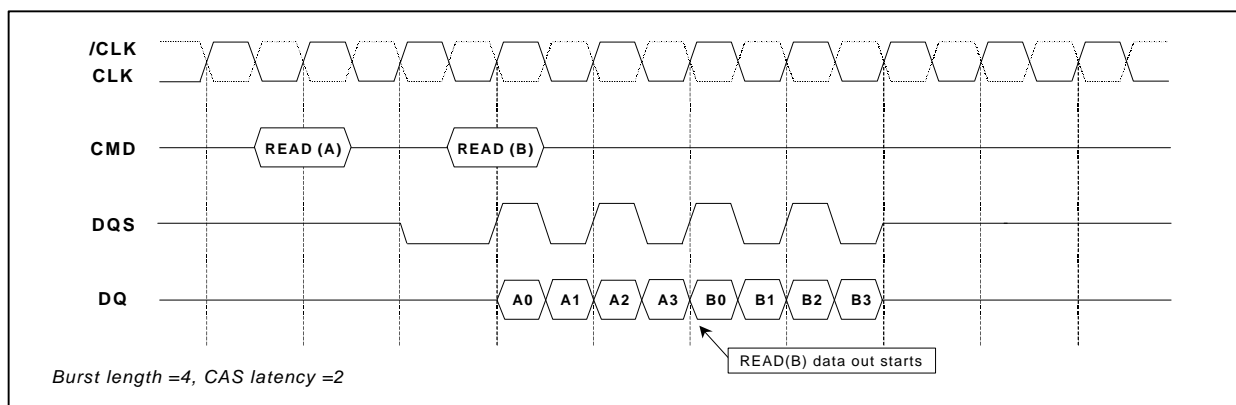
Fig.1. Burst Read and Burst Write



Burst Read followed by Burst Read

Back to back read operation in the same or different bank is possible as shown in Fig.2. Following first Read command, consecutive Read command can be initiated after BL/2 ticks of clock. In other words, minimum earliest possible Read command that does not interrupt the previous read data, can be issued after BL/2 clock is met. When Read(B) data out starts, data strobe signal does not transit to Hi-Z but toggle high and low for Read(B) data.

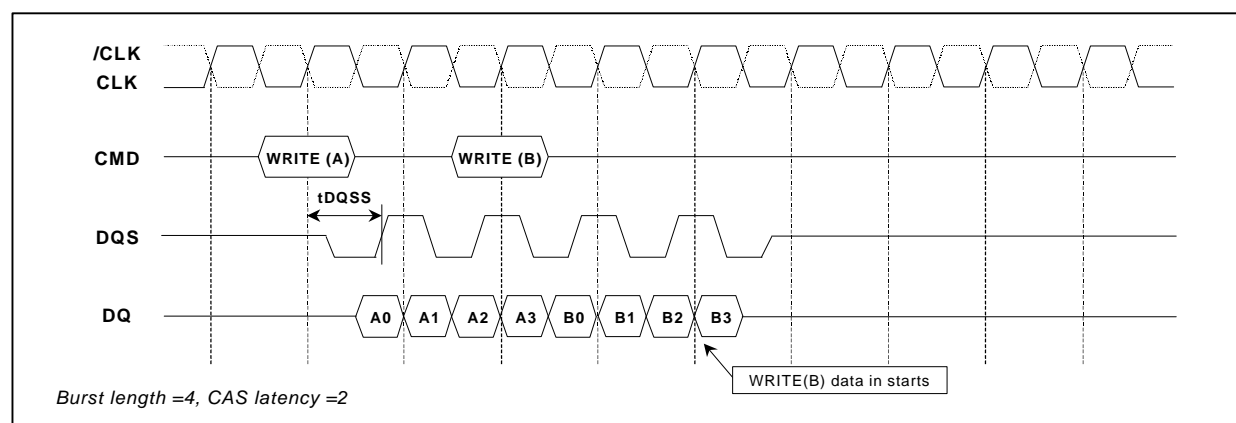
Fig.2. Burst Read followed by Burst Read



Burst Write followed by Burst Write

Back to back write operation in the same or different bank is possible as shown in Fig.3. Following first Write command, consecutive Write command can be initiated after BL/2 ticks of clock. In other words, minimum earliest possible Write command that does not interrupt the previous write data, can be issued after BL/2 clock is met. When Write(B) data in starts, data strobe signal does not transit to Hi-Z but toggle high and low for Write(B) data. Though the timing shown in Fig.3. is based on $t_{DQSS}=0.75 \cdot t_{CK}$, minimum number of clock of BL/2 for back to back write can be applied when $t_{DQSS}=1.25 \cdot t_{CK}$.

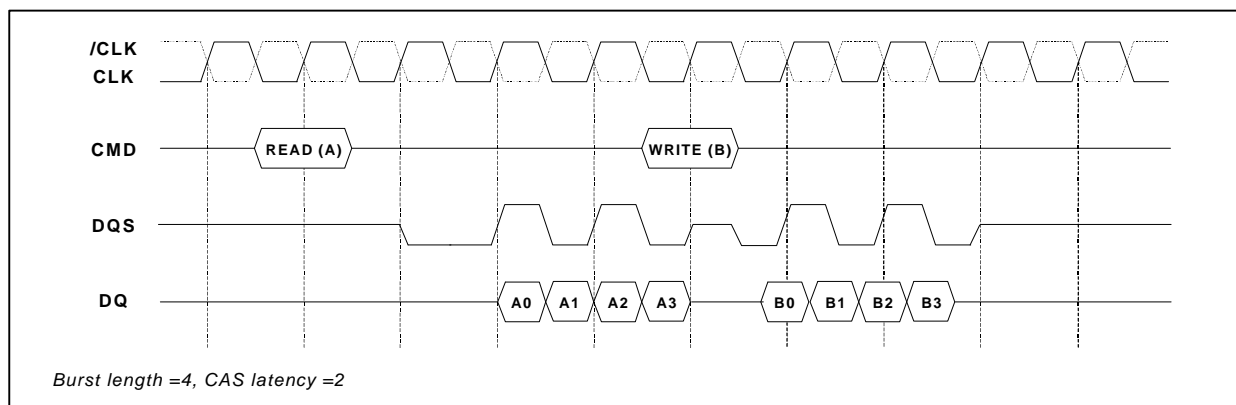
Fig.3. Burst Write followed by Burst Write



Burst Read followed by Burst Write

Back to back read followed by write operation in the same or different bank is possible as shown in Fig.4. Following first Read command, consecutive Write command can be initiated after $\text{RU}\{\text{CL}+\text{BL}/2\}$ ticks of clock. (RU=Round Up for half cycle of CAS latency, such as 1.5 and 2.5). In other words, minimum earliest possible Write command that does not interrupt the previous read data can be issued after $\text{RU}\{\text{CL}+\text{BL}/2\}$ clock is met.

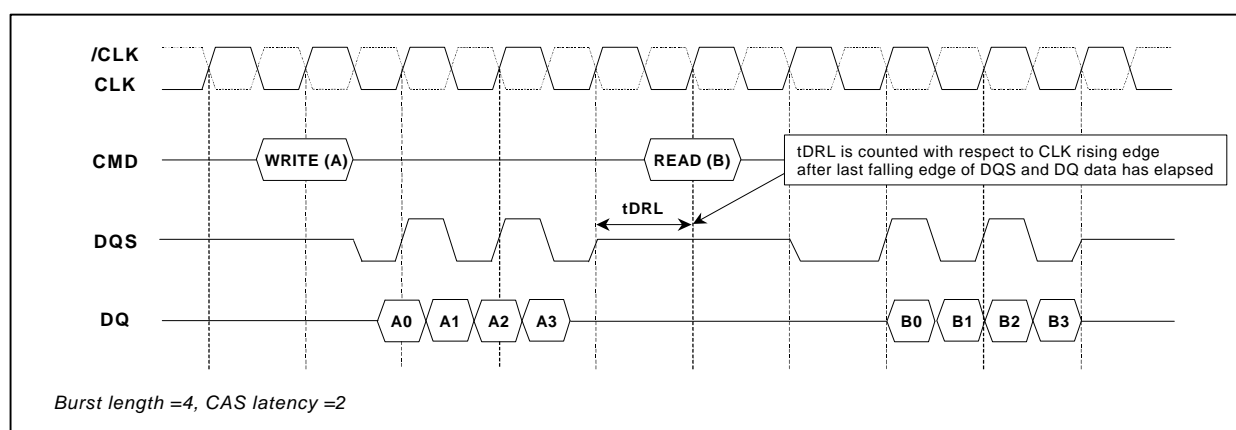
Fig.4. Burst Read followed by Burst Write



Burst Write followed by Burst Read

Back to back write followed by read operation in the same or different bank is possible as shown in Fig.5. Following first Write command, consecutive Read command can be initiated after $(\text{BL}/2+1+\text{tDRL})$ ticks of clock. In other words, minimum earliest possible Read command that does not interrupt the previous write data can be issued after $(\text{BL}/2+1+\text{tDRL})$ clock is met.

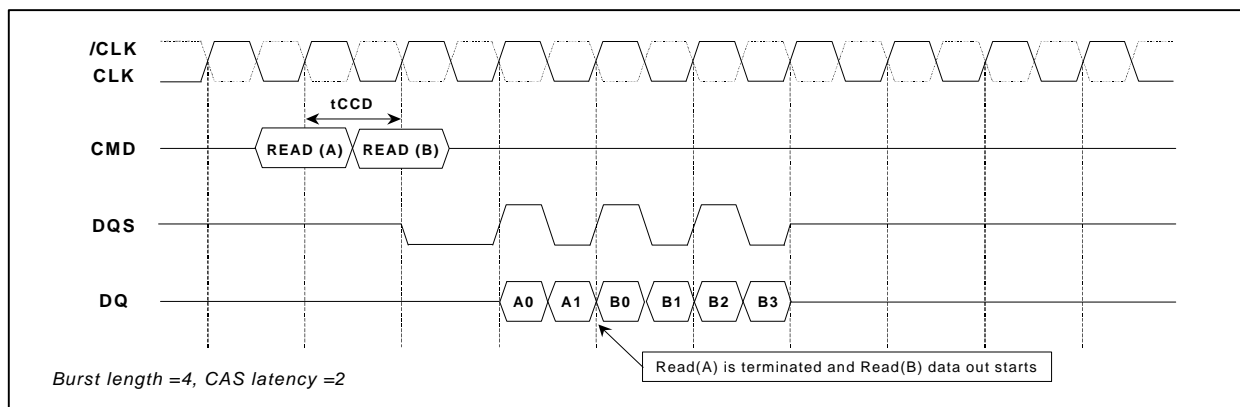
Fig.5. Burst Write followed by Burst Read



Burst Read terminated by another Burst Read

Read command terminates the previous Read command and the data is available after CAS latency for the new command. Minimum delay from a Read command to next Read command is determined by /CAS to /CAS delay (t_{CCD}). Timing diagram is shown in Fig.6.

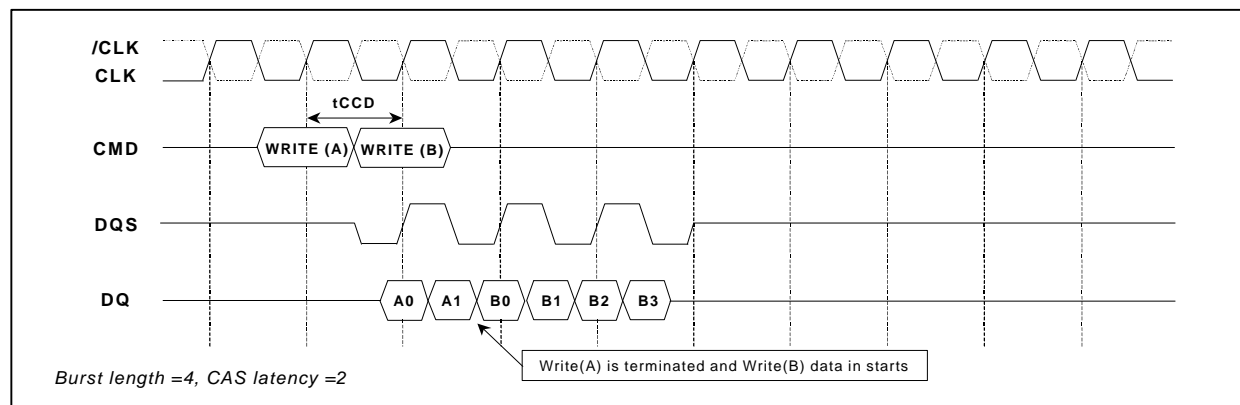
Fig.6. Burst Read terminated by another Burst Read



Burst Write terminated by another Burst Write

Write command terminates the previous Write command and the data is available after CAS latency for the new command. Fastest Write command to next Write command is determined by /CAS to /CAS delay (t_{CCD}). Timing diagram is shown in Fig.7.

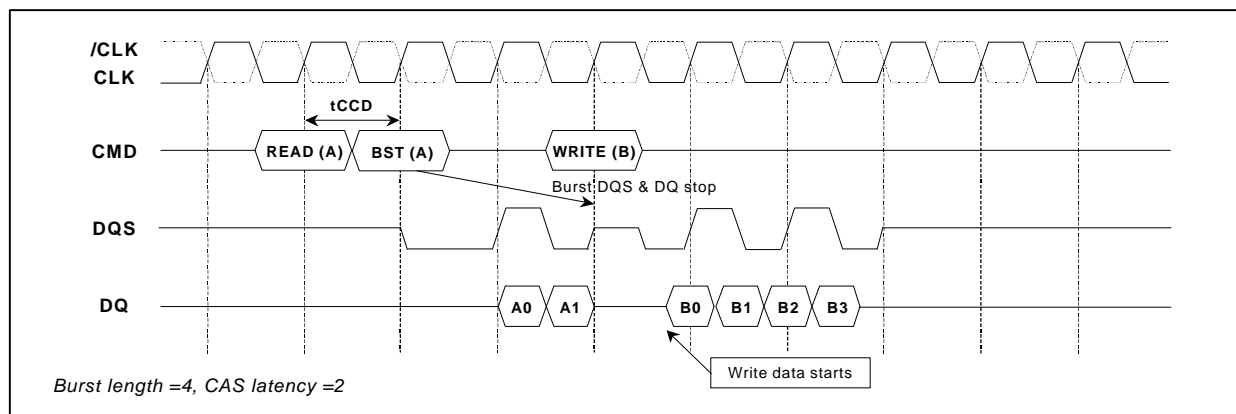
Fig.7. Burst Write terminated by another Burst Write



Burst Read terminated by another Burst Write

Write command terminates the previous Read command with the insertion of Burst Stop command that disables the previous Read command. The Burst Stop command interrupts bursting read data and data strobe signal with the same latency as CAS Latency (CL). The minimum delay for Write command after Burst Stop command is $RU\{CL\}$ clocks irrespective BL. The Burst Stop command is valid for Read command only.

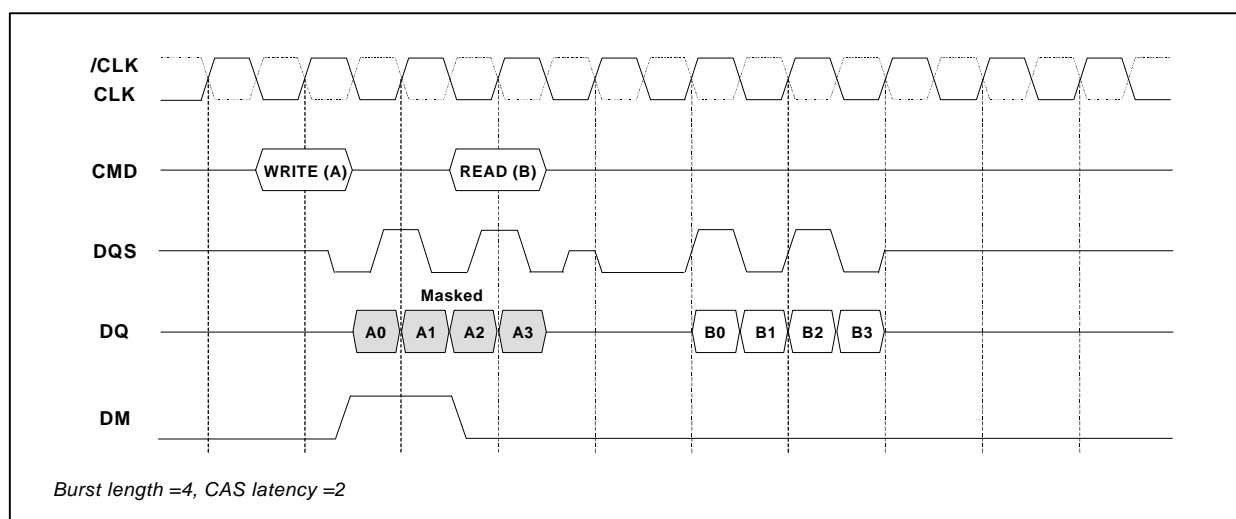
Fig.8. Burst Read terminated by another Burst Write



Burst Write terminated by another Burst Read

Read command terminates the previous Write command and the new burst read starts as shown in Fig.9. The minimum write to read command delay is 2 clock cycle irrespective of CL and BL. If input write data is masked by the Read command, DQ and DQS input are ignored by the DDR SDRAM. It is illegal for a Read command to interrupt a Write with autoprecharge command.

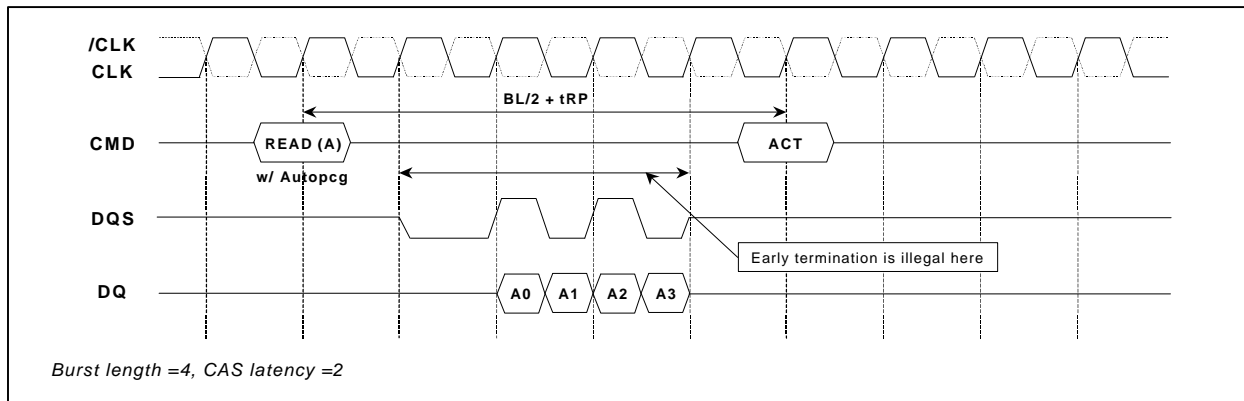
Fig.9. Burst Write terminated by another Burst Read



Burst Read with Auto Precharge

If a Read with Auto Precharge command is detected by memory component in CLK(n), then there will be no commands presented to this bank until CLK(n+BL/2+tRP). Internal precharging action will happen in CLK(n+BL/2).

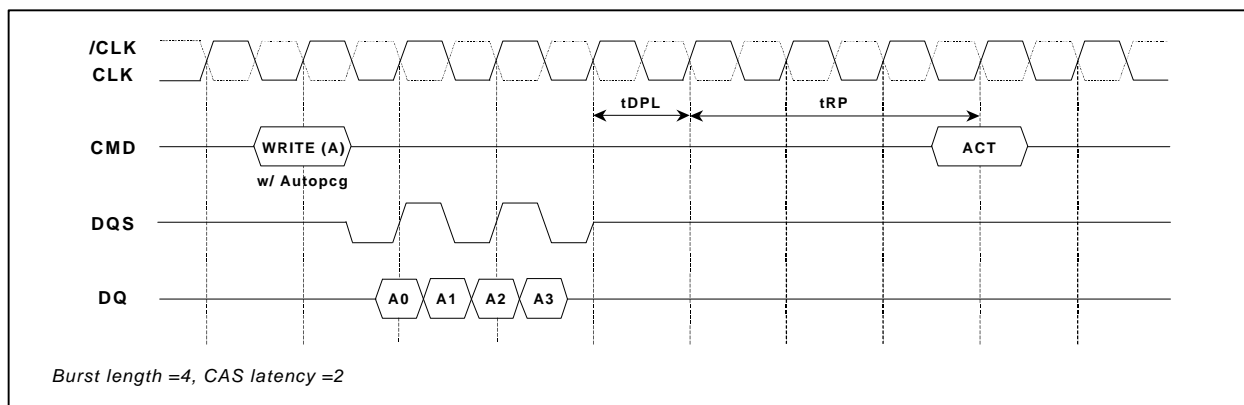
Fig.10. Burst Read with Auto Precharge



Burst Write with Auto Precharge

If a Write with Auto Precharge command is detected by memory component in CLK(n), then there will be no commands presented to this bank until CLK(n+BL/2+1+tDPL+tRP). Last Data in to Precharge delay time (tDPL) is needed to guarantee the last data has been written. tDPL is measured with respect to rising edge of clock where last falling edge of data strobe (DQS) and DQ data has elapsed. Internal precharging action will happen in CLK(n+BL/2+1+tDPL) as shown in Fig.11.

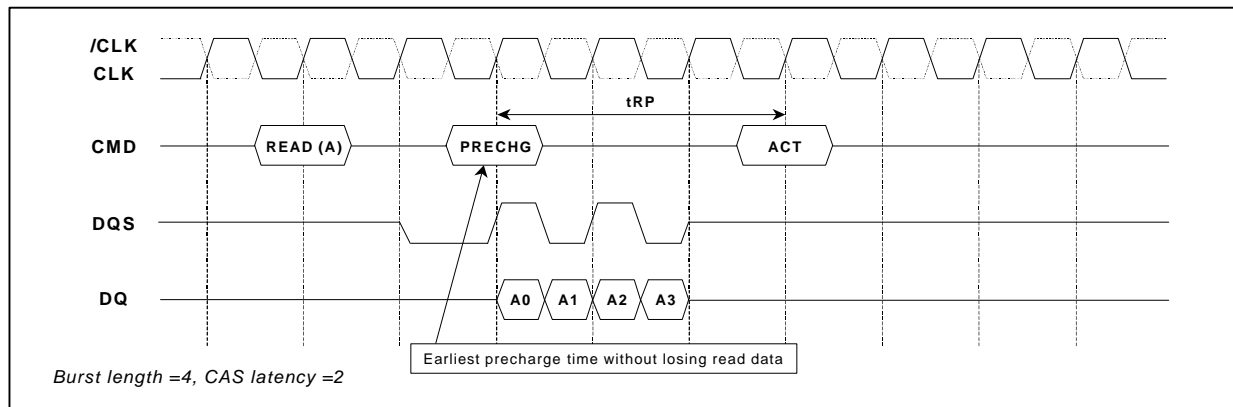
Fig.11. Burst Write with Auto Precharge



Precharge command after Burst Read

The earliest Precharge command can be issued after Read command without the loss of data is $BL/2$ clocks. The Precharge command can be given as soon as t_{RAS} time is met. Fig.12 shows the earliest possible Precharge command can be issued for $CL=2$ and $BL=4$.

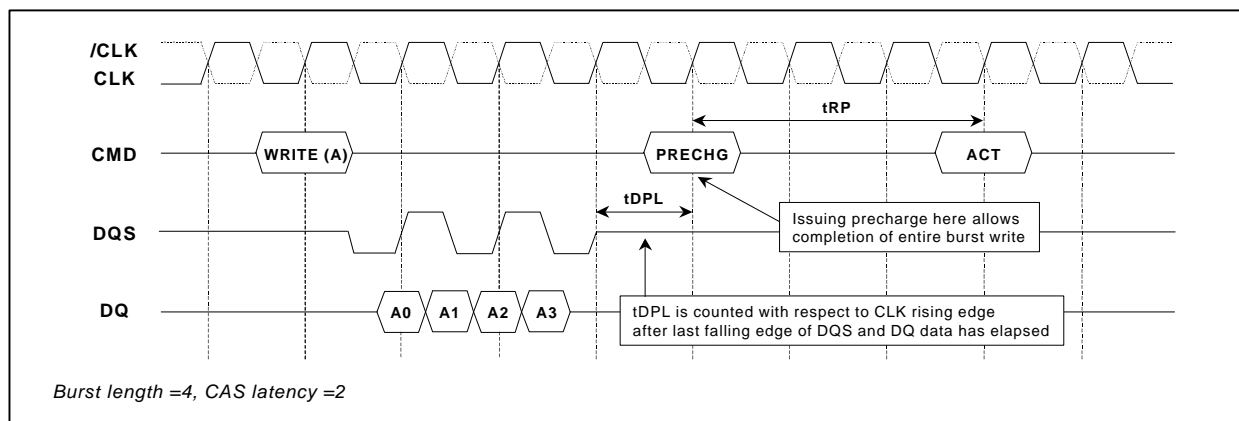
Fig.12. Precharge command after Burst Read



Precharge command after Burst Write

The earliest Precharge command can be issued after Write command without the loss of data is $(BL/2+1+t_{DPL})$ ticks of clocks. The Precharge command can be given as soon as t_{RAS} time is met. Fig.13 shows the earliest possible Precharge command can be issued for $CL=2$ and $BL=4$.

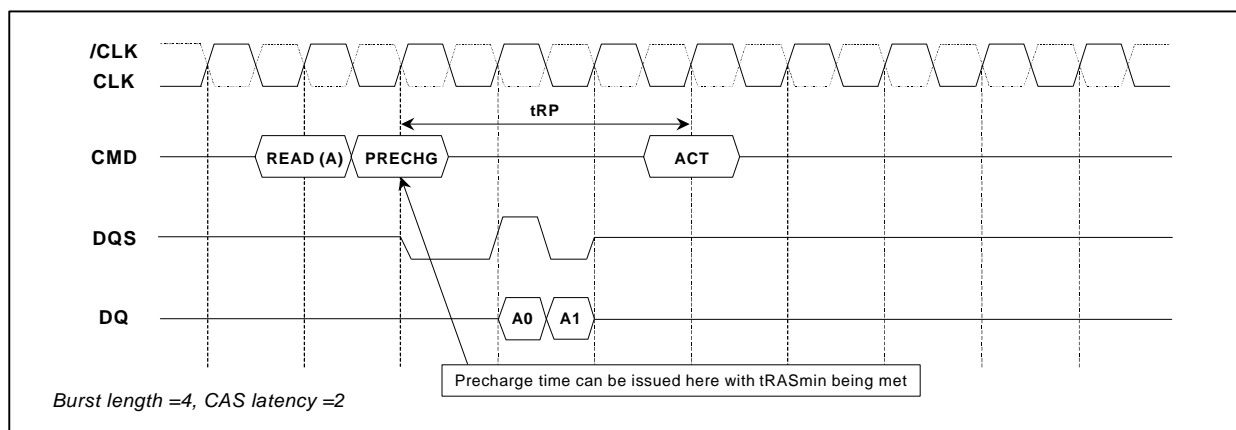
Fig.13. Precharge command after Burst Write



Precharge termination of Burst Read

The Burst Read (with no Autoprecharge) can be terminated earlier using a Precharge command as shown in Fig.14. This terminates read data when the remaining elements are not needed. It allows starting precharge early. The Precharge command can be issued any time after Burst Read command when t_{RASmin} is met. Activation or other commands can be initiated after t_{RP} time.

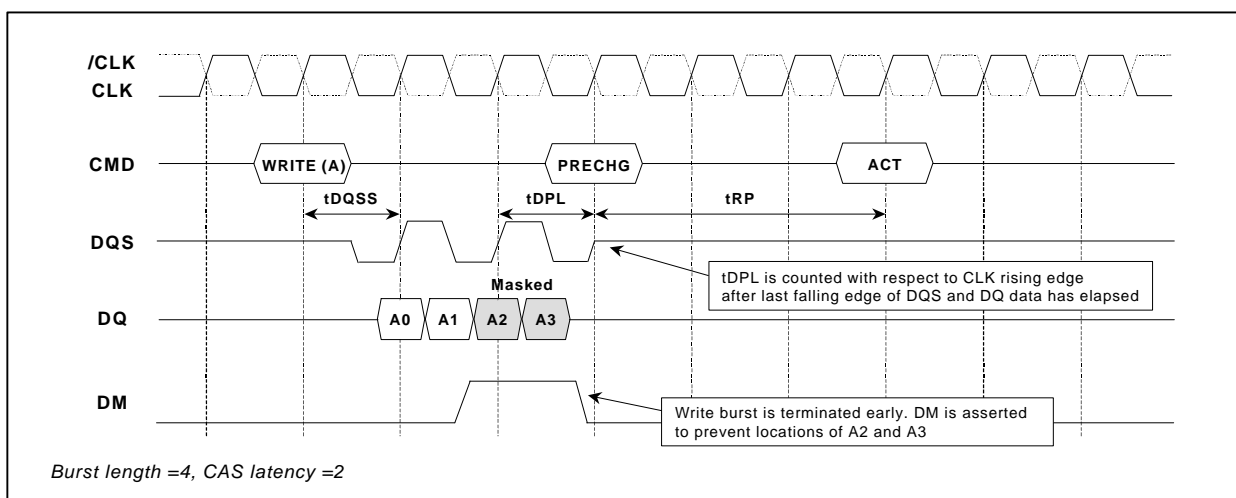
Fig.14. Precharge termination of Burst Read



Precharge termination of Burst Write

The Burst Write (with no Autoprecharge) can be terminated earlier using a Precharge command along with the Write Mask (DM) as shown in Fig.15. This terminates write data when the remaining elements are not needed. It allows starting precharge early. Precharge command can be issued after Last Data in to Precharge delay time (t_{DPL}). t_{DPL} is measured with respect to rising edge of clock where last falling edge of data strobe (DQS) and DQ data has elapsed. DM should be used to mask the remaining data (A2 and A3 for this case). t_{RAS} time must be met to issue the Precharge command.

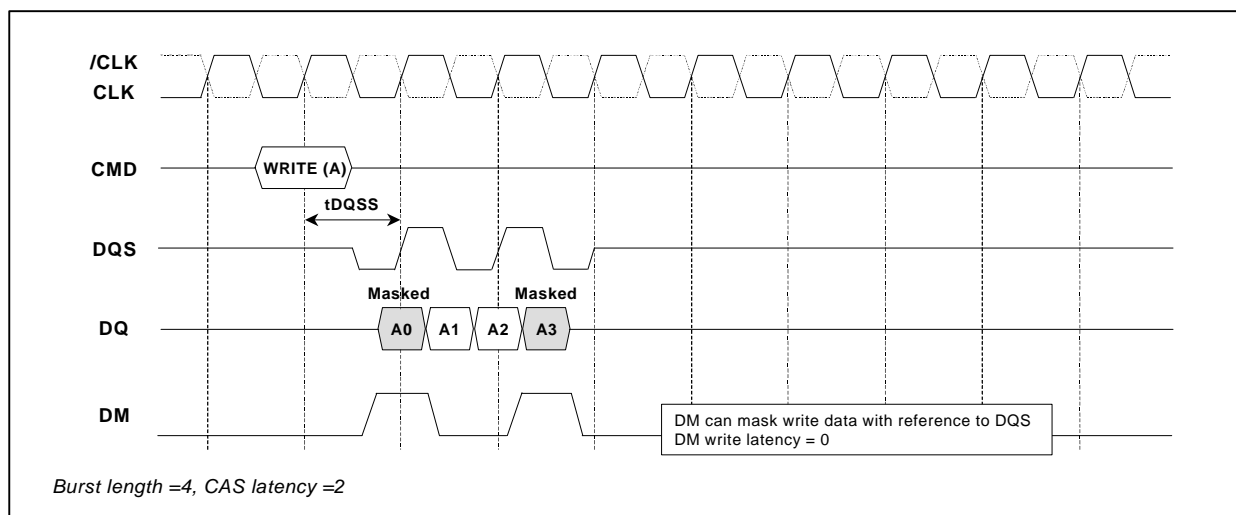
Fig.15. Precharge termination of Burst Write



DM masking (Write)

DM command masks burst write data with reference to data strobe signal and it is not related with read data. DM command can be initiated at both the rising edge and the falling edge of the DQS. DM latency for write operation is zero. For x16 data I/O, DDR SDRAM is equipped with LDM and UDM which control lower byte (DQ0~DQ7) and upper byte (DQ8~DQ15) respectively.

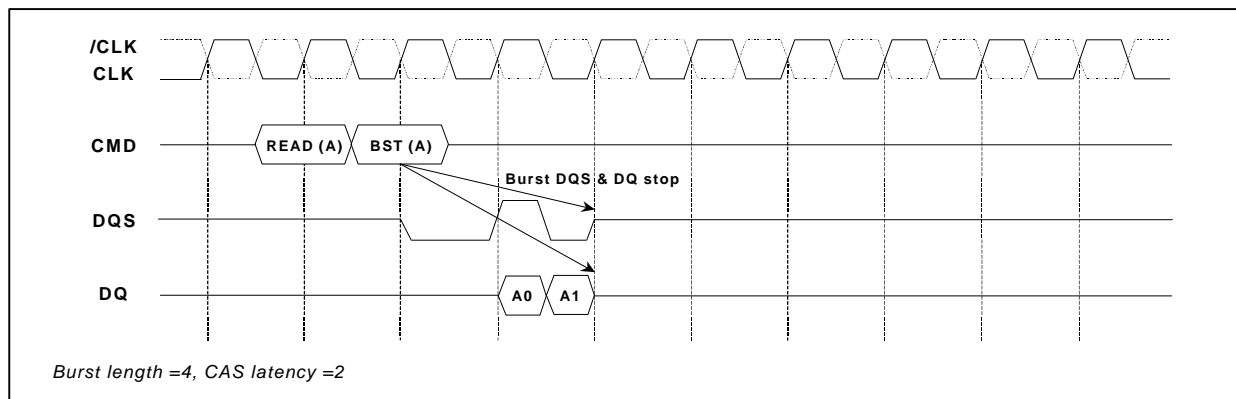
Fig.16. DM masking (Write)



Burst Stop command (Read)

When /CS=L, /RAS=H, /CAS=H and /WE=L, DDR SDRAM enter into Burst Stop mode, which bursts stop read data and data strobe signal with reference to clock signal. BST command can be initiated at the rising edge of the clock as other commands do. BST command is valid for read operation only. BST latency for read operation is the same as CL.

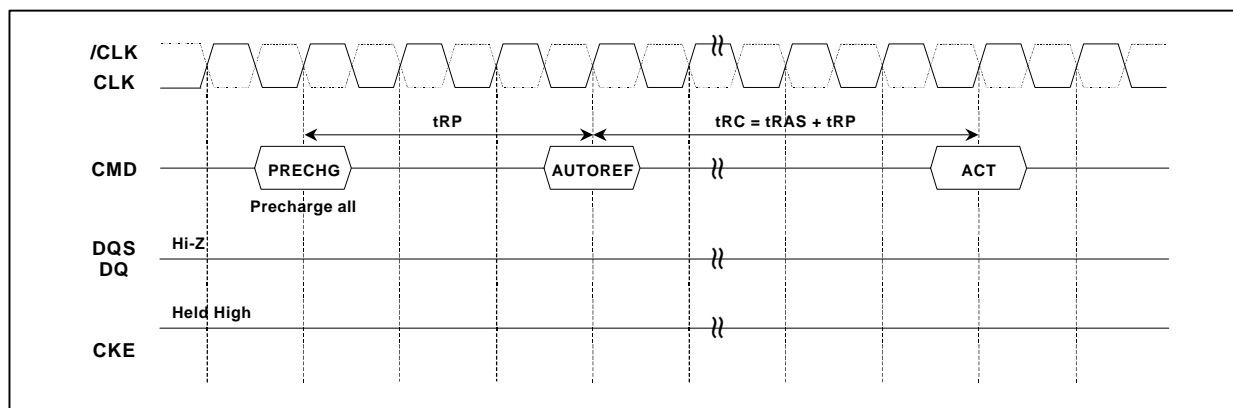
Fig.17. Burst Stop command (Read)



Auto Refresh and Precharge All command

When $/CS=L$, $/RAS=L$, $/CAS=L$ and $/WE=H$, DDR SDRAM enter into Auto Refresh mode, which executes refresh operation with internal address increment. AREF command can be initiated at the rising edge of the clock as other commands do. Before entering Auto Refresh mode, all banks must be in a precharge state and AREF command can be issued after tRP period from Precharge All command.

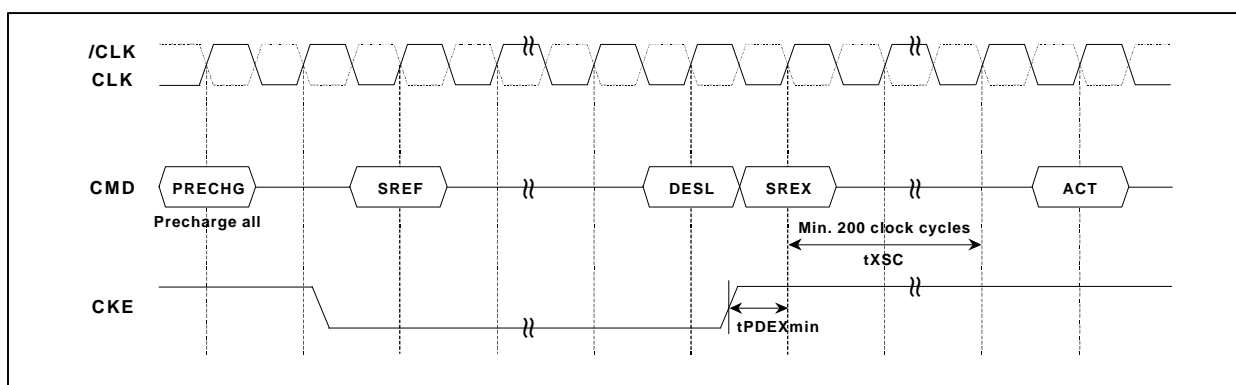
Fig.18. Auto Refresh and Precharge All command



Self Refresh Entry and Exit

When $CKE=L$, $/CS=L$, $/RAS=L$, $/CAS=L$ and $/WE=H$, DDR SDRAM enter into Self Refresh mode, which executes self refresh operation with internal address increment. Before issuing Self Refresh command, all banks must be in a pre-charge state and CKE must be low. SREF command can be initiated at the rising edge of the clock as other commands do. Because the clock buffer and internal DLL circuit are disabled during self refresh state, Self Refresh Exit (SREX) should guarantee the stable input clock. Therefore, a minimum of 200 cycles of stable input clock, where CKE is held high, is required to lock the internal DLL circuit of DDR SDRAM. A minimum $tPDEX$ (Power Down Exit Time) must be met before entering SREX command.

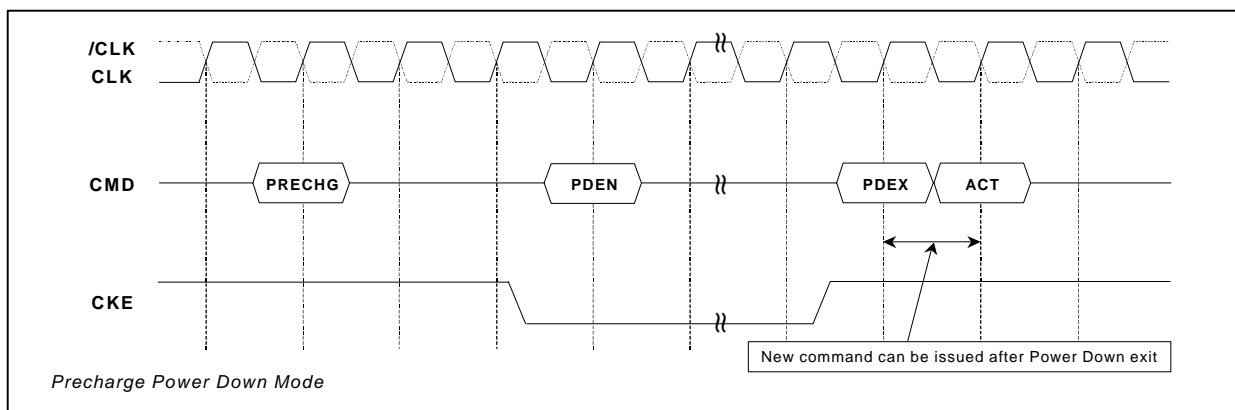
Fig.19. Self Refresh Entry and Exit



Power Down mode

A Power Down mode can be achieved by asserting CKE=L as shown in Fig.20. There are two kinds of Power Down mode: 1. Active and 2. Precharge Power Down mode. The device must be in idle state and all banks must be closed before CKE assertion in Precharge Power Down mode. Active Power Down mode can be initiated in row active state. The device will exit Power Down mode when CKE is sampled high at the rising edge of the clock.

Fig.20. Power Down mode



CKE function

Since clock suspend mode in SDR SDRAM cannot be used in DDR SDRAM, it is illegal to issue CKE=L during read or write burst.

Fig.21. CKE function

