

Technical Note

DDR2 SDRAM Bank Addressing

Introduction

DDR2 SDRAM introduces changes in bank and array architecture along with addressing for improved performance and power. Table 1 on page 3 offers a comparison of number of banks and page size between DDR2 and DDR SDRAM devices. This Technical Note describes the evolution in array architecture from DDR to DDR2 SDRAM.

Array Definition

Page size refers to the minimum number of column locations that are on any row and are accessed with a single ACTIVATE command. This is equal to the number of column locations times the number of DQ on the device. For example, the 512Mb x 8 DDR2 SDRAM has 1,024 column locations. Thus, the page size is 1,024 columns x 8 DQ, which equals 8,192 bits. Dividing the 8,192 bits by a word length of 8 = 1,024 bytes, or 1KB.

Each time an ACTIVATE command is issued, all the bits within the page are read by the sense amplifiers and restored to the correct value; this process is a major contributor to active power consumption. Thus, a smaller pages size leads to lower operating currents.

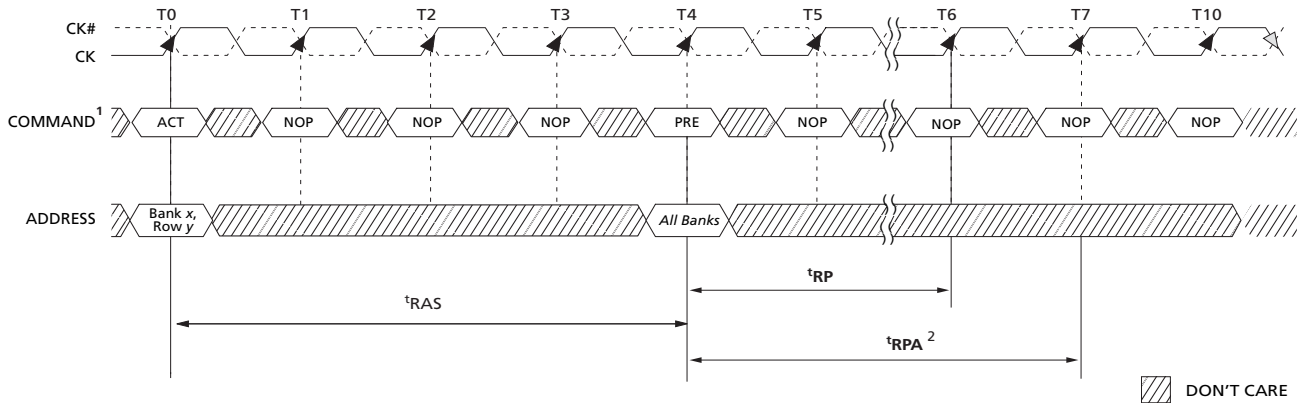
DDR2 specifies page size as 1KB for x4 and x8 configurations of 256Mb–2Gb densities (half of DDR page size), in order to reduce operating currents in these devices. At 512Mb and greater densities, the page size increases to 2KB for x16 DDR2 devices. Although the power consumption of an individual x16 DRAM device will be greater than the x4 or x8 configurations of the same density, the system power consumption will actually be lower, because fewer components are needed to support the typical 64-bit bus width.

DDR2 Bank Access

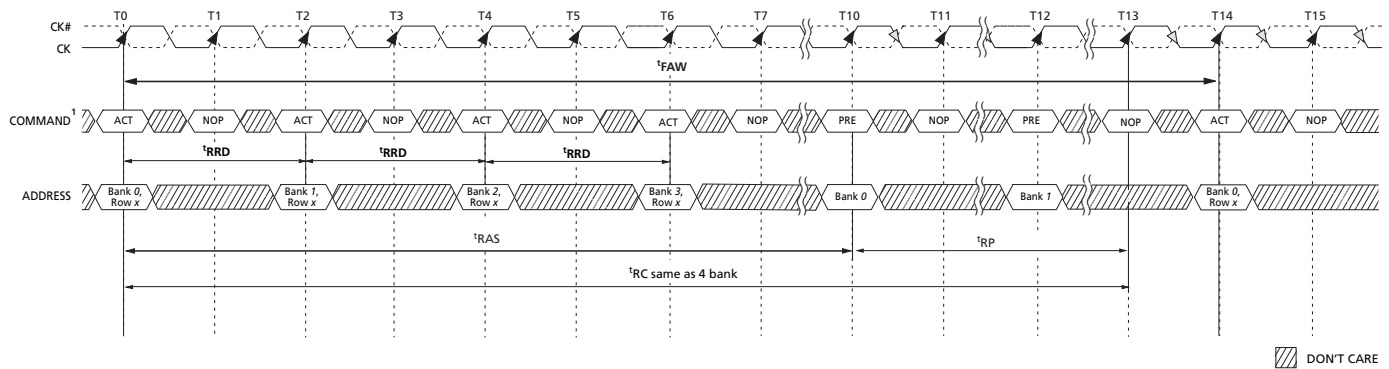
For 1Gb and greater densities, DDR2 specifications increase the number of banks on the device from four to eight to improve system performance (bank interleave and page availability).

A 4-bank DDR2 bank access sequence is similar to DDR, as illustrated in Figure 1. Note that $t_{RRD} = 7.5\text{ns}$ for 1KB page DRAM, but t_{RRD} increases to 10ns for 2KB page size because of the increased power requirements for a larger page size. Once a bank is pre-charged, it may be accessed again after t_{RC} has been satisfied.

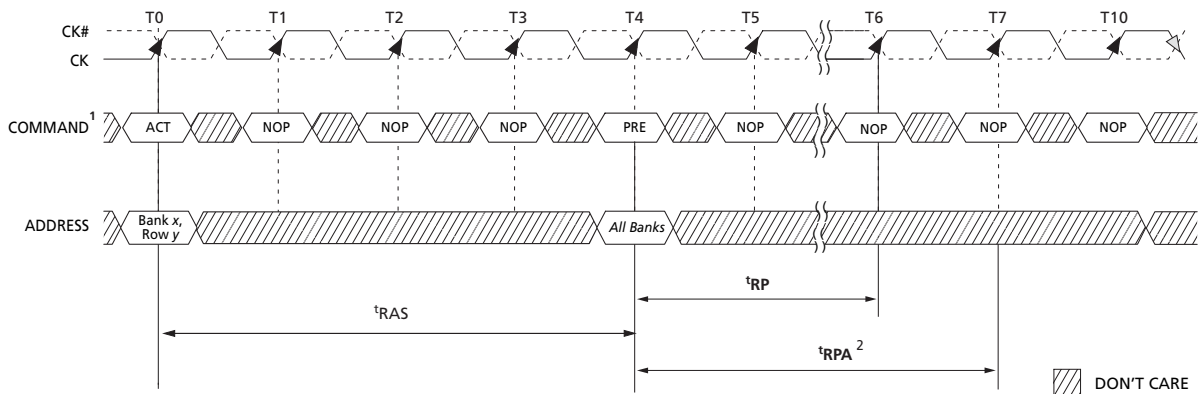
Eight-bank DDR2 offers more flexible ways for the system to access the device, at the cost of increased power consumption. To protect power delivery from affecting DRAM device functionality, only four banks may be accessed within any window of t_{FAW} , as illustrated in Figure 2 on page 2. Also, for a PRECHARGE (ALL) command on the eight bank device, t_{RP} changes to t_{RPA} (t_{RPA} requires one additional clock before the next command may be issued), as shown in Figure 3 on page 2.

Figure 1: Example ACT for 4-Bank Devices


- Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 2. t_{RPA} applies for eight bank devices and anytime one or more banks are open.

Figure 2: Example ACT for 8-Bank Devices


- Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 2. t_{RRD} is 7.5ns on 1KB page size and 10ns on 2KB page size (two-clock minimum).
 3. t_{FAW} is 37.5ns on 1KB page size and 50ns on 2KB page size (two-clock minimum).

Figure 3: Example t_{RP} (4 bank) and t_{RPA} (8 bank)


- Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 2. t_{RPA} applies for eight bank devices and anytime one or more banks are open.

Comparison of SDRAM Architectures

Table 1: DRAM Architectures

Density	Feature	x4	x8	x16
256Mb (4 Bank)	ROW	8K (A0-A12)	8K (A0-A12)	8K (A0-A12)
	BANK	4 (BA0-BA1)	4 (BA0-BA1)	4 (BA0-BA1)
	COLUMN	2K (A0-A9, A11)	1K (A0-A9)	512 (A0-A8)
	PAGE SIZE	1KB	1KB	1KB
512Mb (4 Bank)	ROW	16K (A0-A13)	16K (A0-A13)	8K (A0-A12)
	BANK	4 (BA0-BA1)	4 (BA0-BA1)	4 (BA0-BA1)
	COLUMN	2K (A0-A9, A11)	1K (A0-A9)	1K (A0-A9)
	PAGE SIZE	1KB	1KB	2KB
1Gb (8 Bank)	ROW	16K (A0-A13)	16K (A0-A13)	8K (A0-A12)
	BANK	8 (BA0-BA2)	8 (BA0-BA2)	8 (BA0-BA2)
	COLUMN	2K (A0-A9, A11)	1K (A0-A9)	1K (A0-A9)
	PAGE SIZE	1KB	1KB	2KB
2Gb (8 Bank)	ROW	32 K (A0-A14)	32 K (A0-A14)	16K (A0-A13)
	BANK	8 (BA0-BA2)	8 (BA0-BA2)	8 (BA0-BA2)
	COLUMN	2K (A0-A9, A11)	1K (A0-A9)	1K (A0-A9)
	PAGE SIZE	1KB	1KB	2KB

Conclusion

Optimizing throughput on an 8-bank device is simple if a few key timing parameters are observed. With the introduction of 8 banks ^tFAW, ^tRPA and ^tRRD(x16) have been defined. The 4-bank activate period (^tFAW) restricts the number of ACTIVE commands that can occur within a window of time. The PRECHARGE ALL period (^tRPA) is increased by one clock cycle for any 8-bank device and the ACTIVATE to ACTIVATE period (^tRRDx16) slightly increases the time between active commands to different banks for a 2K page size device.



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This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.